2004-06

Hardware-in-the-Loop control of a cascaded multi-level converter

Barlow, Jacob L.

Monterey, California. Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

HARDWARE-IN-THE-LOOP CONTROL OF A CASCADED MIULTI-LEVEL CONVERTER

by

Jacob L. Barlow

June 2004

Thesis Advisor:	Robert W. Ashton
Second Reader:	Roberto Cristi

Approved for public release; distribution is unlimited

THIS PAGE INTENTIONALLY LEFT BLANK

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.			
1. AGENCY USE ONLY ***(Leave blank)***	**2. REPORT DATE** June 2004	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE: Hardware-in-the-Loop Control of a Cascaded Multi-Level Converter			**5. FUNDING NUMBERS**
6. AUTHOR(S) Jacob L. Barlow			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000			**8. PERFORMING ORGANIZATION REPORT NUMBER**
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A			**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited			**12b. DISTRIBUTION CODE**

13. ABSTRACT (maximum 200 words)

Next-generation U.S. Navy destroyers, known as DD(X), will use electric drive motors to meet their propulsion needs instead of the traditional mechanical drives. The use of electric drive motors in naval vessels has spurred the development of high power converters. This thesis examines the feasibility of using an advanced control algorithm known as Sine-triangle Pulse Width Modulation (SPWM) in combination with a Cascaded Multi-Level Converter (CMLC) in order to meet the U.S. Navy's strict requirements. The SPWM control algorithm was designed in Simulink and experimentally tested on a CMLC previously constructed at the Naval Postgraduate School. The controller and converter successfully powered a quarter horsepower three-phase induction motor.

14. SUBJECT TERMS DC-AC, Multi-Level, Cascaded Multi-Level, Converter, Inverter, Sine-Triangle, Space Vector Modulation, dSPACE, IPS, DD(X)			**15. NUMBER OF PAGES** 83
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UL

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

THIS PAGE INTENTIONALLY LEFT BLANK

Approved for public release; distribution is unlimited

HARDWARE-IN-THE-LOOP CONTROL OF A CASCADED MULTI-LEVEL CONVERTER

Jacob L. Barlow
Ensign, United States Navy
B.S., North Carolina State University, 2003

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 2004

Author: Jacob L. Barlow

Approved by: Robert W. Ashton
Thesis Advisor

Roberto Cristi
Second Reader

John P. Powers
Chairman, Department of Electrical and Computer Engineering

THIS PAGE INTENTIONALLY LEFT BLANK

ABSTRACT

Next-generation U.S. Navy destroyers, known as DD(X), will use electric drive motors to meet their propulsion needs instead of the traditional mechanical drives. The use of electric drive motors in naval vessels has spurred the development of high power converters. This thesis examines the feasibility of using an advanced control algorithm known as Sine-triangle Pulse Width Modulation (SPWM) in combination with a Cascaded Multi-Level Converter (CMLC) in order to meet the U.S. Navy's strict requirements. The SPWM control algorithm was designed in Simulink and experimentally tested on a CMLC previously constructed at the Naval Postgraduate School. The controller and converter successfully powered a quarter horsepower three-phase induction motor.

THIS PAGE INTENTIONALLY LEFT BLANK

TABLE OF CONTENTS

LIST OF FIGURES

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF TABLES

THIS PAGE INTENTIONALLY LEFT BLANK

EXECUTIVE SUMMARY

The United States Navy is becoming increasingly interested in the use of electric drive propulsion for their next generation of ships. Past and present research projects such as the Integrated Power System (IPS) and the DD(X) program have led to positive results. These positive results have encouraged the U.S. Navy to continue development of their electric drive technology. In addition to research and development by the U.S. Navy, the commercial maritime industry realized the advantages of electric drive propulsion years ago and subsequently has already made the switch to the all-electric ship design. This radical change in commercial ship design has led to a plethora of electric drive motors and auxiliary components.

The basic concept behind the all-electric ship design is that all the power generated aboard the ship is produced in the form of electrical energy. This design deviates from current naval design because both mechanical and electrical power is generated aboard the ship. The mechanical power is used to propel the ship, while the electrical power is used to power all of the ship's service loads. In contrast the all-electric ship design will use electric drive motors in combination with high power converters to meet the ship's propulsion and service needs.

One of the major components necessary for the U.S. Navy to complete the transition to the all-electric ship is the high power converter used to operate the electric drive motor. Unlike typical commercial converters, the converter used for naval applications must produce a high fidelity output current. This high fidelity output current is necessary in order to meet the U.S. Navy's strict acoustic performance standards.

A promising converter topology known as the Cascaded Multi-Level Converter (CMLC) is capable of meeting the U.S. Navy's power conversion needs. The CMLC connects a multi-level converter to each end of a load. Each multi-level converter develops a specified voltage, and their difference is the amount of voltage that is applied to the load. Figure E-1 illustrates the schematic diagram of a three-phase CMLC capable of producing nine output voltage levels.

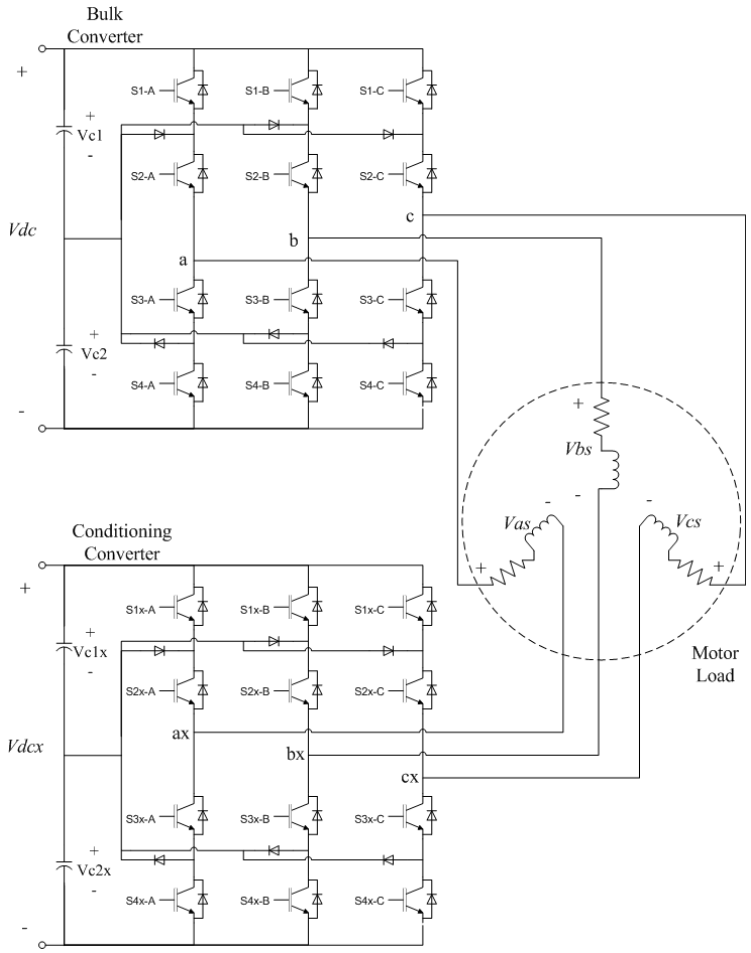

Figure E-1. Nine Level CMLC Schematic

The CMLC in Figure E-1 uses a series of Insulated Gate Bipolar Transistors (IGBT) to act as switches. With the proper switching sequence, a sinusoidal voltage and current output can be produced.

The two most popular switching algorithms for the CMLC are Space Vector Modulation (SVM) and Sine-triangle Pulse Width Modulation (SPWM). SVM allows for closed-loop control systems to be developed, but is also more complex in design and implementation. SPWM can only be used as an open-loop control system, however it has the advantage of being easier to design and implement.

SPWM was chosen for the switching algorithm used to control the CMLC constructed at the Naval Postgraduate School (NPS) as part of a previous thesis. SPWM uses a reference sine wave compared to a series of triangle waveforms. This comparison es-

sentially creates a digitized version of the reference sine wave. The comparison of the reference waveform to the triangle waveforms can be seen in Figure E-2. The digitized sine wave output can be seen in Figure E-3.

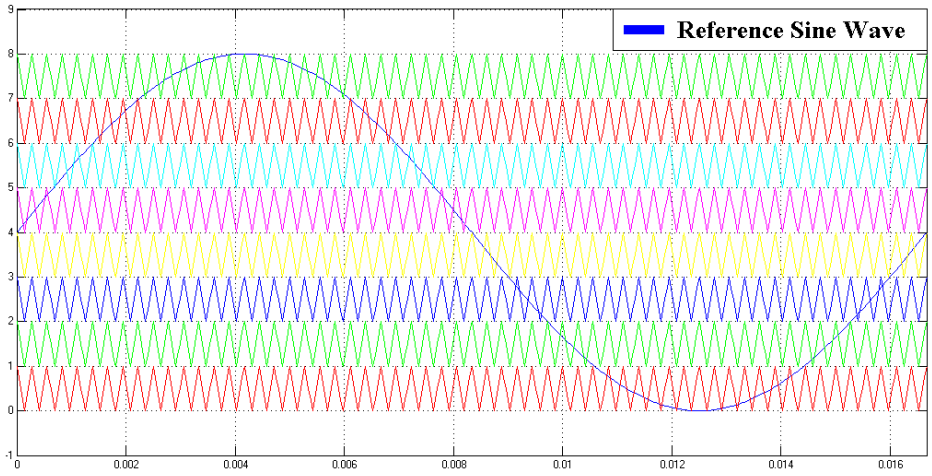

Figure E-2. SPWM Comparison

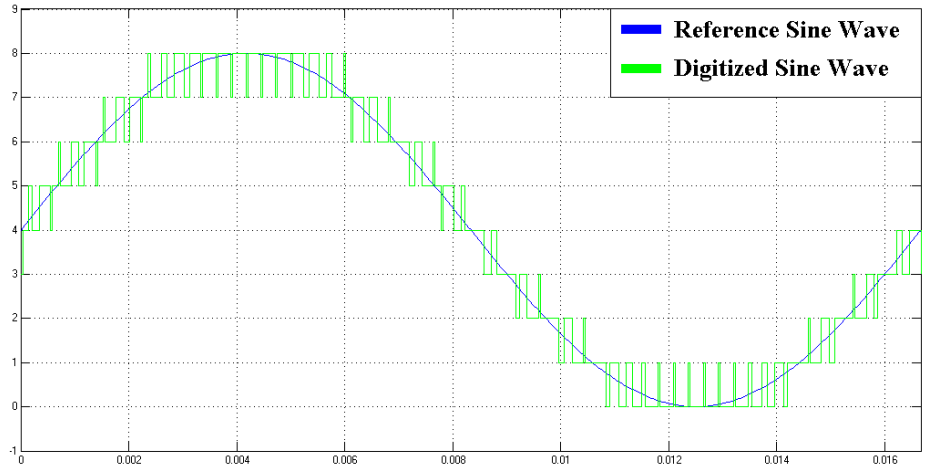

Figure E-3. Digitized Sine Wave

The digitized waveform (green) in Figure E-3 is used to determine which switch configuration is necessary to create the desired output voltage level. The algorithm was developed in Simulink and interfaced with the hardware using a Digital Signal Processor (DSP) card made by dSPACE.

With the use of Simulink and dSPACE, Rapid Control Prototyping (RCP) and Hardware-In-the-Loop (HIL) simulation were possible. The basic idea behind RCP is control algorithms can be developed and tested without the use of expensive and labor

intensive hardware development. HIL simulation allows for the control algorithm to be interfaced with real hardware that would otherwise be difficult to simulate in a program such as Simulink.

The control algorithm developed for this thesis was applied to the CMLC constructed at NPS. In order to accommodate the DSP card interface, the CMLC was modified. Modifications included a new layout, digital logic input terminals, and a delay circuit.

After extensive hardware and software performance analysis, the converter was proven to operate according to theory and similar experimental results. Figure E-4 illustrates the three-phase current waveforms produced using an induction motor load.

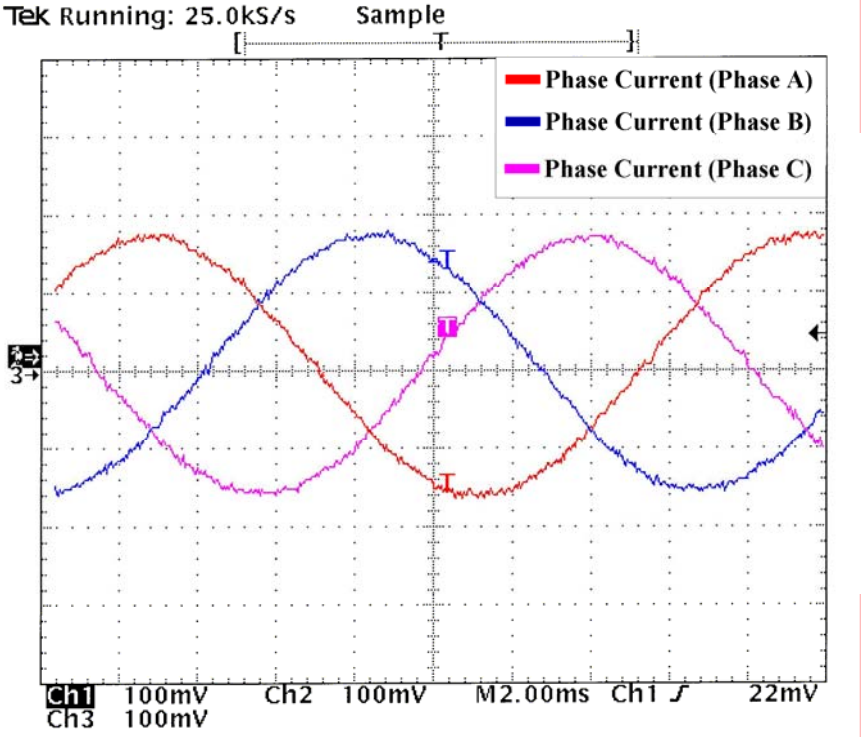

Figure E-4. Three-Phase Current Waveforms

As can be seen from Figure E-4, the output of the CMLC consists of three sinusoidal current waveforms that contain minimal distortion. The goal of this thesis was to show that the CMLC is an ideal candidate for use as the high power converter in the new all-electric ship design.

I. INTRODUCTION

A. NAVAL POWER REQUIREMENTS

Currently the U. S. Navy is investigating electric drive propulsion for use aboard next-generation destroyers. The change from mechanical drive propulsion to electric drive propulsion may seem like a new direction in naval ship construction; however, the concept has been implemented several times since the early twentieth century [1]. In fact, the first aircraft carrier to join the U. S. Fleet was propelled using electric drive [2]. The switch from mechanical to electric drive has been done and undone several times due to the relative advantages of the two drive methods.

In the early twentieth century, the limits imposed by the manufacturing and processing of steel and other materials used to make gears and various components for mechanical drive systems forced the U.S. Navy to turn to electric drive in order to meet its propulsion needs. Years later, as the processing of metals was refined, the advantages again changed hands, and mechanical drive became the staple of U.S. Naval vessels. After several more switches between mechanical and electric drive, mechanical systems gained a considerable following, thus producing the fleet currently in service [1].

Once again the U.S. Navy stands at the crossroads of mechanical and electric drive propulsion. The same technological revolution that brought about modern features such as sonar, radar, and computer navigation now promises new and exotic weapons such as lasers and rail guns. In order to accommodate these new weapons systems, the generation and distribution of electrical power aboard ship must be dramatically improved [3].

Electrical power consumption has grown significantly over the past few decades, thus stretching the ship's resources to their limits. This growth in power consumption is illustrated in Figure 1 by the increase in electrical power generation aboard U.S. Navy Destroyers from the late nineteenth century to the present.

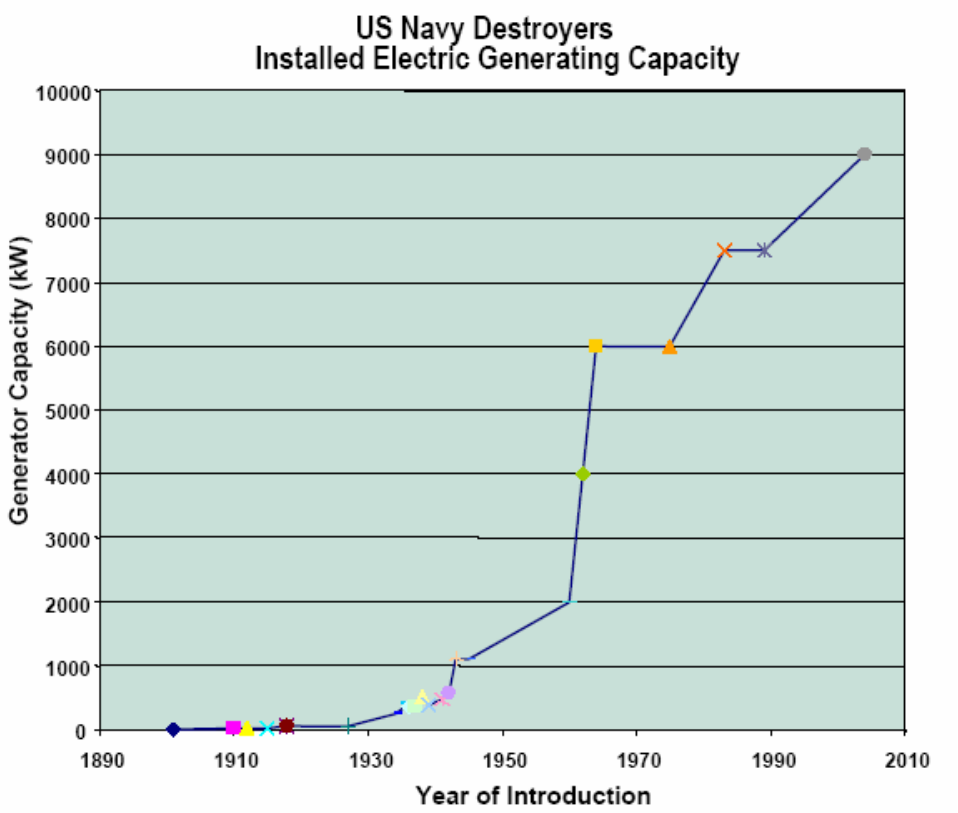

Figure 1. Electric Power Generating Capacity [From Ref. 4.]

As can be seen from Figure 1, the electrical power generating capabilities of destroyers has increased by nearly ten-fold since World War II. This trend directly reflects the power consumption. Since there is limited space aboard ship, a radical design change is required in order to meet the needs of future combat vessels.

The solution to the limited ship's resources comes from switching to electric drive and changing the power distribution system to take advantage of this switch [3]. Figure 2 illustrates the current production and distribution of mechanical and electrical power aboard ships.

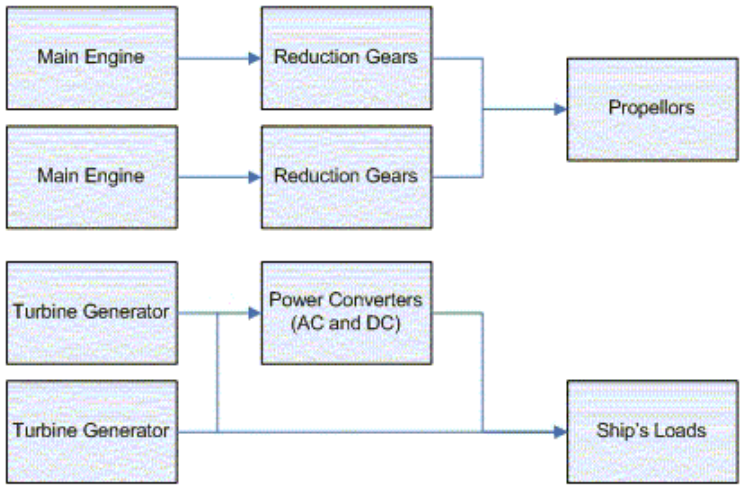

Figure 2. Current Power Production and Distribution

As shown in Figure 2, two separate systems are used to generate and distribute mechanical and electrical power. The limitation of this production and distribution scheme is that the mechanical power generation cannot be used for electrical power production and vice versa.

In order to overcome this limitation, the Naval Surface Warfare Center (NSWC) in Philadelphia, PA has recently completed testing of a system known as the Integrated Power System (IPS). IPS is a full-scale prototype of a proposed power generation and distribution system. Figure 3 illustrates the design tested at IPS.

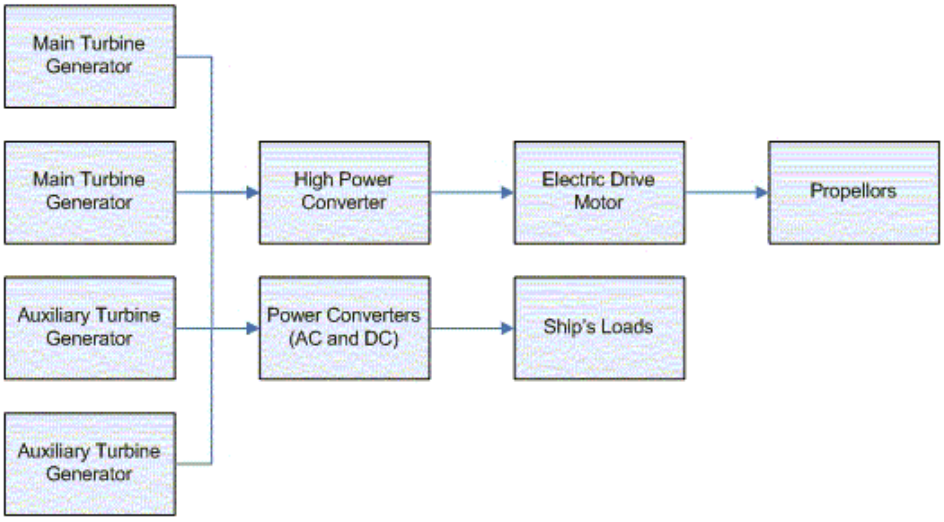

Figure 3. Future Power Production and Distribution

As shown in Figure 3, IPS uses two main turbine generators and two auxiliary turbine generators to produce all the power aboard the ship [3]. Depending on the power demands of the ship, any combination of the four turbines can be used. The different configurations can be seen in Figure 4. The vertical scale is the power required by the ship in watts. The horizontal scale is the speed of the ship in knots. The curved line represents a typical profile of power versus speed for a destroyer. The colored boxes denote the turbine generator configurations that will allow the ship to meet the requirements set forth by the power versus speed profile.

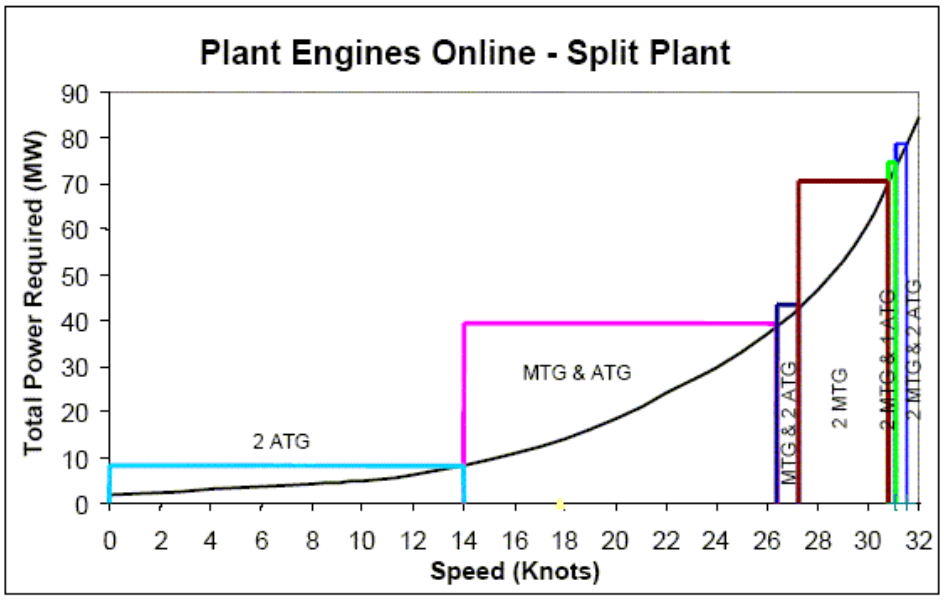

Figure 4. Turbine Generator Configurations for IPS [From Ref. 4.]

The configurability of the turbine generators shown in Figure 4 has two main advantages. First, this system improves the fuel efficiency of the ship. It is important to note that the electric drive technology under investigation by the U.S. Navy is not more efficient than the mechanical drive systems currently in use. However, the fuel efficiency is increased from closely matching the electric power production with the electric power consumption. Additionally, the system was designed to be especially efficient for typical operation of U.S. Navy destroyers. Since the average cruising speed of U.S. Navy destroyers is between 12-14 knots, this system was designed to generate the required power for the propulsion and hotel loads using only the two auxiliary turbine generators. Second, it allows for all of the power produced to be distributed to any system aboard the

ship. For example, when using a rail gun, the majority of the power produced would be devoted to the weapons system. However, if the ship was not currently using any weapons, the available power would be used for propulsion and hotel loads.

The goal of IPS was to determine the feasibility of electric drive propulsion and rapidly reconfigurable power generation. While the research was conducted at the Land Based Engineering Site (LBES), results of this initial trial will aid the design of the next-generation U.S. Navy destroyers known as the DD(X). Additionally, IPS investigated the practicability of using products developed by the commercial industry for use in military applications. The following section will discuss commercial developments in electric drive propulsion.

B. COMMERCIAL ELECTRIC DRIVE SYSTEMS

The commercial maritime industry has made the switch to electric drive propulsion due to the numerous advantages of electric drive over mechanical drive. The following list illustrates the key features that the commercial industry requires of its power plant and propulsion systems.

- Low Cost
- High Fuel Efficiency
- High Reliability
- Low Maintenance
- Compact Design
- Passenger Comfort

Electric drive is capable of exceeding mechanical drive in all of these categories with the use of podded propulsion [5]. Podded propulsion packages the motor and required auxiliary equipment into a compact design known as a *pod*. Figure 5 shows an example of a commercially available pod.

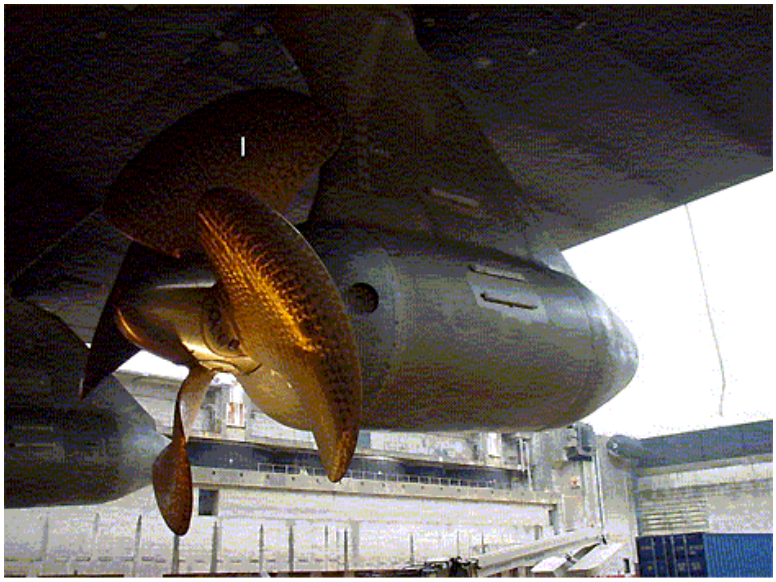

Figure 5. ALSTOM 20MW Azimuth Pod (Mermaid™) [From Ref. 5.]

Podded propulsion, like the one shown in Figure 5, dramatically improves the efficiency of the propulsion motor by creating an optimum undisturbed flow of water to the propeller [5]. Additionally, this undisturbed water flow decreases noise and vibration, thus improving passenger comfort [5]. Podded propulsion also increases the payload capacity of the ship by removing the bulky engine from within the hull and placing it on the outside of the ship [5].

While podded propulsion certainly adds to the advantages of electric drive systems, electric drive in general has a few inherent advantages over mechanical drive. Perhaps most importantly of these inherent advantages is the reduction in the number of moving parts. Moving parts typically have lower reliability and higher maintenance requirements than non-moving parts. Since electric drive systems require fewer moving parts, they typically have a higher reliability and lower maintenance requirements. Another advantage is the configurability of power production and distribution previously discussed.

In addition to podded propulsion, the commercial industry has made significant improvements to the motor drive assemblies used to power the pods. Commercial maritime interest in high wattage power conversion has spurred a plethora of motor drive designs. Because these drives were developed by the commercial industry, cost played an

important role in their design and performance. The following section will provide more details about the different converter topologies.

C. SOLID STATE POWER CONVERSION

Development of the different converter topologies is due for the most part to the commercial maritime industry. However, solutions for the commercial industry will not necessarily work for military applications. Because cost is a paramount concern for the commercial industry, the performance of commercial converters often suffers. In addition to the high reliability and low maintenance that the commercial industry requires, the military also requires its converters to be compact (without the use of pods), battle hardened, and high fidelity.

With the use of podded propulsion, the commercial industry has been able to reduce the amount of equipment inhaul, therefore freeing more space for passengers or cargo. Unfortunately, the U.S. Navy has decided not to pursue development into podded propulsion. This means that in order to increase the amount of space inhaul, the design of the motor and motor drive assemblies must be made as compact as possible. In addition to making the converters compact, the design must also be able to with stand extreme conditions.

U.S. Naval vessels operate under some of the most severe conditions that any ship could ever operate. All the forces of nature, such as temperature, corrosion, and waves, continually act to degrade the ship and its components. In addition to all the natural forces naval vessels are exposed to, ships also face long operational commitments and the extreme conditions a ship is exposed to during a battle. In order for components to survive battle conditions they must withstand a high degree of shock and vibration.

One of the best ways for U.S. Naval vessels to gain an advantage in battle is to identify the enemy without allowing themselves to be identified. Since propulsion motors add a lot of noise to the water, they can be used to identify ships. Despite the fact that motors are often built using similar designs, slight differences in construction can lead to noticeable differences in the noise output of the motor. When a motor is powered by a low fidelity current, torque pulsations are produced. Torque pulsations cause the

motor to vibrate, thus producing an identifiable sound signature. High fidelity converters can dramatically reduce the amount of torque pulsations by eliminating current harmonics. A detailed description of current harmonics will be covered in Chapter V.

This section will introduce the different converter topologies available to convert DC power into AC power. The advantages and disadvantages for each converter topology must be weighed in order to select the optimal converter to meet the U.S. Navy's requirements.

1. Synchro-Converter

Synchro-Converters are used to drive a synchronous motor from an AC bus. Two naturally commutated thyristor converters are joined by a DC link [6]. One converter acts as a rectifier, establishing the voltage on the DC link. The second converter acts as an inverter, taking the DC link voltage and transforming it back into an AC voltage. While converter designs vary, typical input frequencies range from 30 to 200 Hz [6].

Since synchro-converters use thyristor-based converters, they are capable of handling high power motor loads. Additionally, thyristor-based converters are known to be extremely robust.

The commercial industry has made the synchro-converter one of the most commonly used converter topologies. For example, the podded motor in Figure 5 uses a synchro-converter to drive the motor. Unfortunately for the U.S. Navy, synchro-converters produce large current harmonics thus creating torque pulsations.

2. Cycloconverter

Cycloconverters are very similar to synchro-converters except they are designed to operate with induction motors as well as synchronous motors. Cycloconverters do not require the establishment of a DC link; instead they operate directly off of the AC line-frequency input. Cycloconverters can typically produce output frequencies up to 30% of the input line-frequency [7].

Like the synchro-converter, cycloconverters are often constructed using thyristors, thus allowing the cycloconverter to be robust. Cycloconverters are very practical for low-speed, large horsepower applications.

Unfortunately, cycloconverters produce large current harmonics. Additionally, since the converter operates directly off the AC line-frequency input, instead of establishing a DC link, considerable supply-side harmonics are created.

3. Hybrid Converter

Hybrid converters encompass a large class of relatively new designs. Hybrid converters typically combine a six-step, low fidelity converter, with a high fidelity conditioning inverter. This combination allows for the majority of the work to be done by the low fidelity converter, while the conditioning inverter shapes the output into a sinusoidal waveform.

The Naval Postgraduate School (NPS) is developing its own hybrid converter. This converter uses a bulk converter to develop a six-step voltage output. A hysteresis controller then attempts to make up the difference between the square-wave output and a reference sine wave.

Hybrid converters show great potential for being used in medium to high power applications in the future. However, a significant amount of design and testing needs to be performed in order for a full scale hybrid converter to be considered for U.S. Naval applications.

4. Pulse Width Modulation Converter

The converter that was used at LBES in Philadelphia, PA for the IPS program was a Pulse Width Modulation (PWM) Converter. The converter uses an array of H-bridges to create an AC voltage from a DC bus. AC voltages are produced by switching between two DC voltages. The H-bridges are controlled using PWM [3].

While the IPS prototype is considered a success in many areas, power quality was a concern. Both supply side and load side harmonics were larger than predicted. Reducing these harmonics is a goal for future testing of electric drive propulsion.

5. Multi-level Converter

H-bridge converters are actually a type of multi-level converter. Multi-level converters use a DC bus and capacitors to develop *n* number of voltages [8]. Switches are placed between one of the *n* voltage levels and the load. With the use of a proper control algorithm, the converter will develop an *n*-level AC output. More voltage levels means

that a controller can better approximate a reference sine wave. Sinusoidal outputs are desired due to the low harmonic content. Additionally, since the AC output is achieved using many small voltage changes, switching losses and motor stress are reduced.

Multi-level converters are a viable alternative to the simple H-bridge converter used in IPS. In fact, the current design for the DD(X) includes the use of a multi-level converter [4].

6. Cascaded Multi-level Converter

The Cascaded Multi-level Converter (CMLC) is an improvement to the multi-level converter. To create a CMLC, two multi-level converters are connected to the two ends of a load. One converter acts as a bulk converter, supplying the majority of the power to the load. The second converter acts a conditioning converter, supplying harmonic content to transform the square wave output of the bulk converter into a sinusoidal load voltage [9].

With the use of a CMLC, extremely high fidelity currents can be developed in the load. This means that load harmonics are nearly eliminated, thus producing very quiet motors. Additionally, the CMLC can be designed to be extremely robust. The CMLC shows great promise for use by the U.S. Navy and therefore will be the focus of this thesis.

D. THESIS GOAL

The goal of this thesis was to demonstrate that a high fidelity load current can be produced by a CMLC when controlled by the proper algorithm. Completed work and products from this thesis will augment the technical resources of the NPS Power Systems Laboratory and support future thesis projects directed by NAVSEA 05 resource sponsors.

E. THESIS OVERVIEW

Chapter II describes the operation of a CMLC. Chapter III describes popular algorithms used to control CMLCs. Chapter IV provides a detailed account of how the control strategy was implemented using the equipment available at NPS. Chapter V gives the results of experiments run on the CMLC at NPS. Chapter VI discusses the implications of the research done in this thesis, as well as provides ideas for follow-on work at NPS. Appendix A contains the pin configuration table that was used to connect the CMLC to the CP1103 I/O board.

THIS PAGE INTENTIONALLY LEFT BLANK

II. OVERVIEW OF CASCADED MUTLI-LEVEL CONVERTERS

A. PURPOSE

This chapter provides a description of the different types of CMLCs available. Additionally, this chapter discusses the basic operation of the CMLC.

B. DESCRIPTION OF A CASCADED MULTI-LEVEL CONVERTER

The CMLC has become a popular converter for medium- to high-power applications. CMLCs combine a high-power bulk converter with a low-power conditioning converter [9]. The AC output is produced from a DC bus with the use of switches and capacitors. The switch can be any fully controllable power electronic switching device. A popular switch is the Insulated Gate Bipolar Transistor (IGBT). IGBTs combine the fast switching and voltage control of the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) with the high current, high power capability of the Bipolar Junction Transistor (BJT). The number of switches and capacitors required depends upon the specifications of the load.

There are four major parameters that need to be taken into account when designing a CMLC. The first parameter is the number of phases required to power the load. The second parameter is the number of voltage levels to be obtained. The third parameter is the switch configuration. The final parameter is the ratio of the bulk converter's input DC voltage to that of the conditioning converter.

1. Number of Phases

The number of phases required is dictated by the motor load. Typically, motor loads operate using three phases; however, five, seven, or even fifteen phases are not at all uncommon. In fact, IPS uses a fifteen-phase induction machine that is being powered as three separate five-phase systems. Additionally, single-phase converters can be created.

As with many converter topologies, all the phases of the CMLC are identical in construction [7]. The only difference between the phases is the sequence in which the switches are fired. In order for multi-phase systems to work properly, identical switches

on each phase must be fired at different times depending on the displacement angle. The displacement angle is simply 360° divided by the number of phases in the system. For example, a balanced three-phase system has a displacement angle of 120°.

The design of single-phase systems differs slightly from that of multi-phase systems. In both systems, a neutral point is required in order to achieve the different voltage levels. In single-phase systems, the neutral points of the upper and lower converters must be connected. This fact was discovered experimentally and will be explained in Chapter V. In multi-phase systems, the neutral points of the upper and lower converters are not connected.

2. Number of Voltage Levels

The number of voltage levels determines how closely the converter output can approximate a sine wave. By increasing the number of voltage levels, a sine wave can be better approximated [9]. As the output becomes more sinusoidal, the harmonic content of the phase current will decrease [9].

Two numbers are used to indicate the number of voltage levels for a CMLC. The first number refers to the number of voltage levels that the bulk converter is capable of creating. The second number refers to the number of voltage levels the conditioning converter is capable of producing. For example, a CMLC created by connecting two three-level converters to the terminals of a load is referred to as a 3/3 CMLC. It is important to note that the number of voltage levels for the bulk converter does not necessarily have to equal the number of voltage levels of the conditioning converter.

The total number of voltage levels achievable is simply the product of the number of voltages levels for each converter. For example, a 3/5 CMLC is capable of producing fifteen different voltage levels. Certain voltage level combinations are common because of their ease of implementation; however, there is no standard number of voltage levels.

3. Switch Configuration

The switch configuration refers to how the source voltage is applied to each individual switch. The most popular configuration is known as Neutral-Point Clamped (NPC) [9]. NPC switches only have a fraction of the DC input voltage applied across it.

When using NPC switches, the voltage applied to each switch is reduced. This means that for a given system, lower rated switches can be used. On the other hand, for a given switch rating, the DC bus voltage of the system can be increased.

4. Input DC Voltage Ratio

The ratio of the input DC voltages of the bulk and conditioning converters can have a significant effect on the operation of the CMLC [9]. In order to understand the effect this ratio can have it is necessary to transform the phase voltages into the *quadrature-direct* (*q-d*) reference frame. Reference frames are used to transform a nonlinear system into a linear system for a specific quiescent or operating point. For more information on the *q-d* reference frame please refer to Reference [10]. The first step of this transformation is to represent the phase voltages in terms of the line-to-neutral point voltages of the converters:

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_a - v_{ax} \\ v_b - v_{bx} \\ v_c - v_{cx} \end{bmatrix}. \tag{2.1}$$

The line-to-neutral point voltages in Equation 2.1 are now used to represent the phase voltages in the *q-d* reference frame by means of the following equations:

$$v_{qs} = \frac{2}{3}\left(v_{as} - \frac{1}{2}v_{bs} - \frac{1}{2}v_{cs} \right) \tag{2.2}$$

and

$$v_{ds} = \frac{1}{\sqrt{3}}\left(v_{cs} - v_{bs} \right). \tag{2.3}$$

Equations 2.2 and 2.3 allow all possible combinations of the phase voltages to be represented in the *q-d* reference frame. Once the transform is complete, it is interesting to look at a vector plot for all the combinations. Figure 6 illustrates the effect of different voltage ratios on the performance of a 3/3 CMLC.

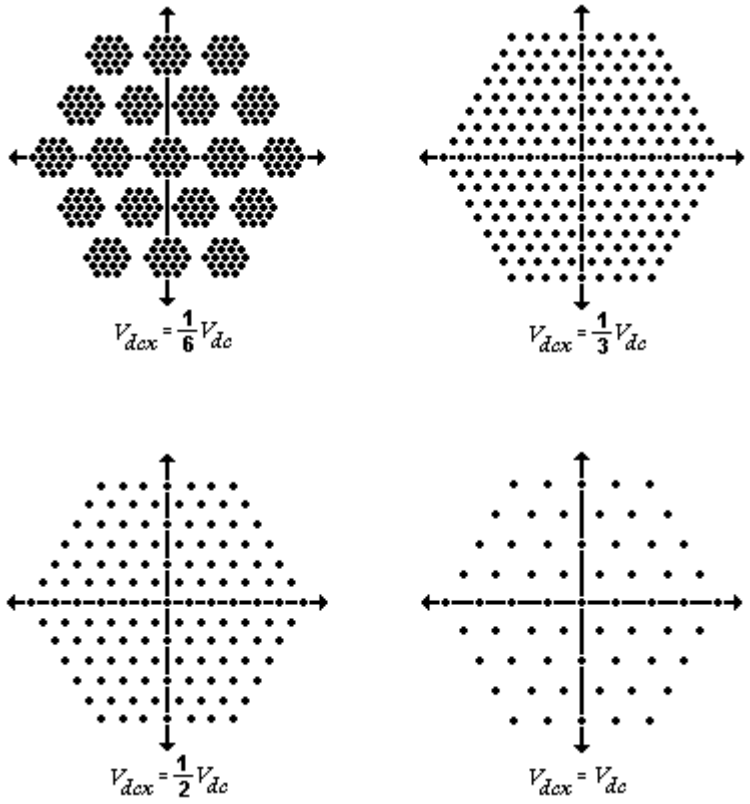

Figure 6. 3/3 CMLC Voltage Vector Plot [From Ref. 9.]

The voltages V_{dc} and V_{dcx} in Figure 6 refer to the DC bus voltage of the bulk and conditioning converters, respectively. Each point on the plots in Figure 6 represents a unique voltage output of the system. The voltage output of the system depends upon the instantaneous configuration of the switches in both of the converters for all three phases [9]. As the number of switching states increases, a sine wave can be better approximated. From the four plots it can be seen that the most unique switching states occurs when the ratio of the bulk and conditioning converter input DC voltage is 3:1.

C. OPERTION OF A CASCADED MULTI-LEVEL CONVERTER

The CMLC constructed at NPS is a nine-level, three-phase, NPC CMLC. Since this is the converter design that this thesis is based upon, it will be used in this section to explain the operation of a CMLC. Figure 7 shows a schematic of the 3/3 CMLC constructed at NPS.

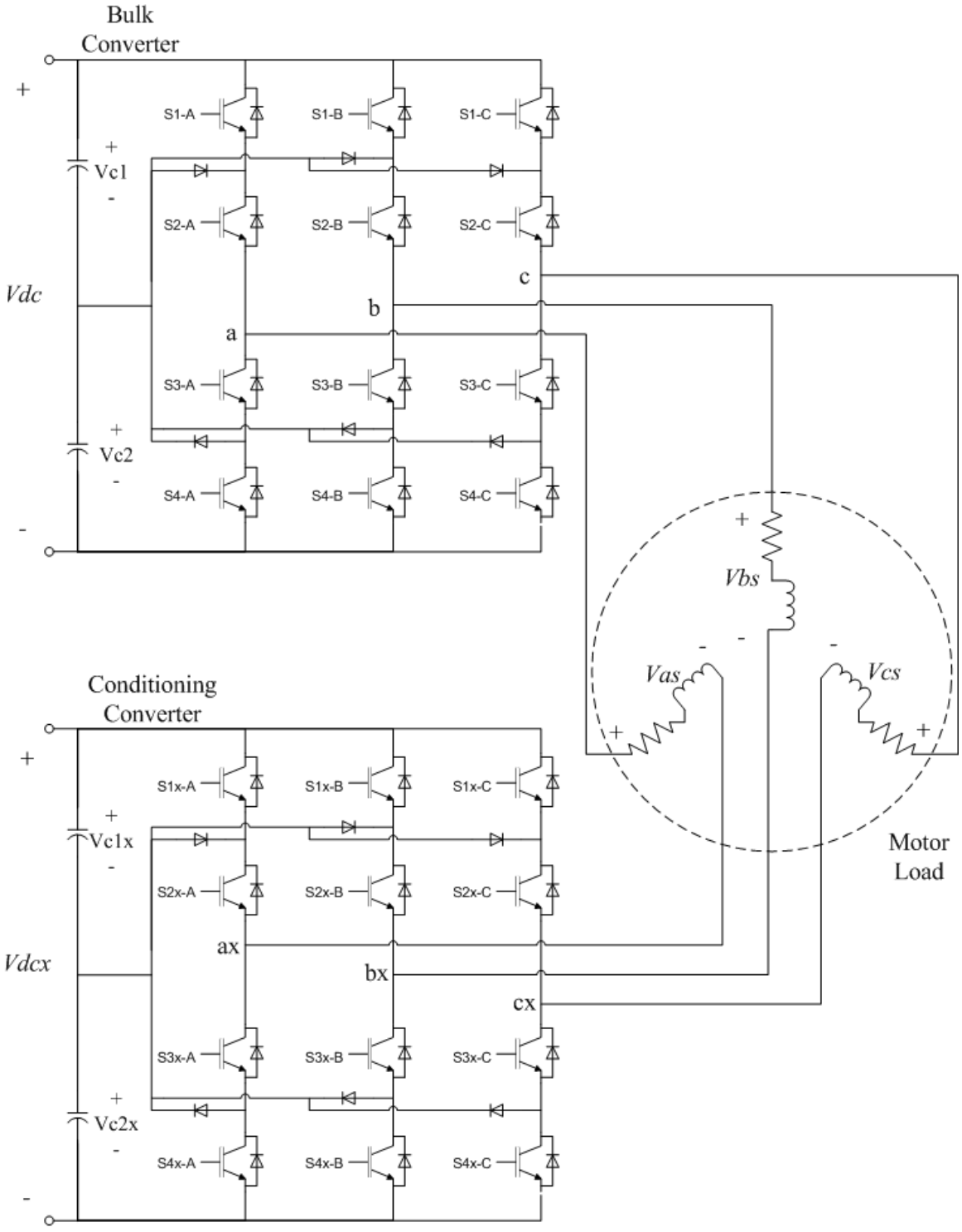

Figure 7. 3/3 CMLC Schematic Diagram

As can be seen in Figure 7, the bulk converter consists of three sets of four switches. Each set of switches can be controlled to produce one of three voltages. The

conditioning converter's construction is identical to that of the bulk converter. The motor load is a quarter horsepower three-phase induction motor.

The different voltage levels are achieved by turning certain pairs of switches on or off [9]. Table 1 shows all the possible switch configurations and their corresponding output for the "A" phase.

S1	S2	S3	S4	S1x	S2x	S3x	S4x	a	ax	a − ax
1	1	0	0	0	0	1	1	3·E	−E	4·E
1	1	0	0	0	1	1	0	3·E	0	3·E
1	1	0	0	1	1	0	0	3·E	E	2·E
0	1	1	0	0	0	1	1	0	−E	E
0	1	1	0	0	1	1	0	0	0	0
0	1	1	0	1	1	0	0	0	E	−E
0	0	1	1	0	0	1	1	−3·E	−E	−2·E
0	0	1	1	0	1	1	0	−3·E	0	−3·E
0	0	1	1	1	1	0	0	−3·E	E	−4·E

Table 1. Switch Configurations and Outputs for Phase A

The first eight columns in Table 1 represent the eight different switches located in the "A" phase of the CMLC in Figure 6 (S1-A through S2-A and S1x-A through S4x-A). A "1" in the column denotes that the switch has been fired, in other words, the switch is on. A "0" in the column denotes that the switch has not been fired, in other words, the switch is off. The "a" and "ax" columns express the output of the bulk and conditioning converters, respectively. The final column indicates the voltage applied to the "A" phase of the motor, where "E" is simply the value of V_{dcx}.

A simple control algorithm can be used to demonstrate how the different voltage levels can be used to approximate a sine wave. The algorithm steps through the different voltage levels in order to approximate the sine wave. Figure 8 illustrates the voltage waveform created using this simple algorithm.

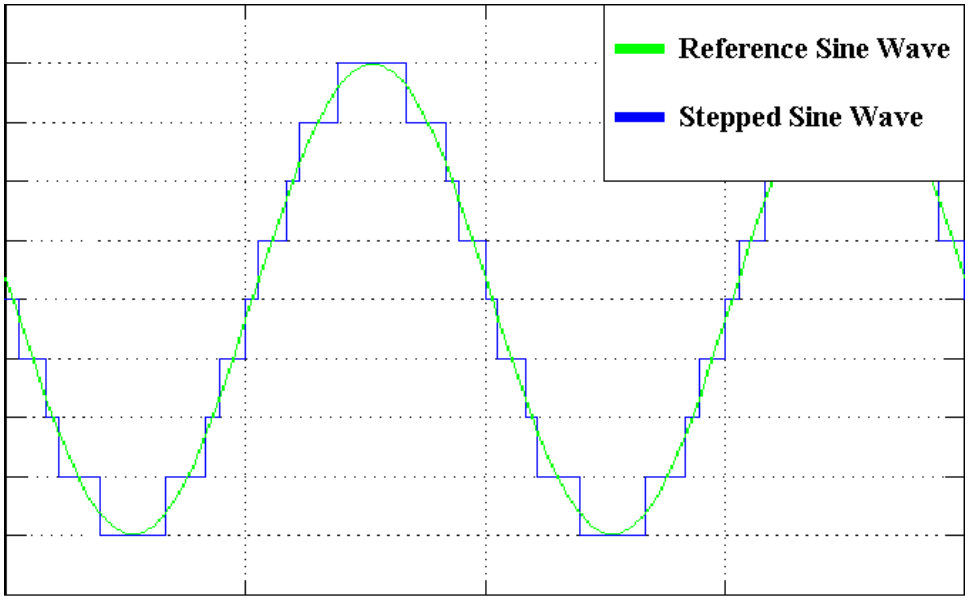

Figure 8. Nine-Level Sine Wave Approximation

The reference sine wave (green) can be seen in Figure 8. Also, the nine-level step approximation (blue) can be seen in Figure 8. If the number of voltage levels was decreased, then the approximation would not be as good. If the number of voltage levels was increased, then the approximation would be better.

For a given number of voltage levels, the approximation can be made better using more advanced control algorithms. These control algorithms may take more effort to implement, but the reduction in output current and voltage harmonics is significant. The next chapter discusses two of the most popular advanced control algorithms.

D. SUMMARY

The CMLC is used to transform a DC bus voltage into an AC sinusoidal output voltage. The CMLC accomplishes this task by connecting different DC input values to the load using a set of switches. Load requirements dictate the design of the CMLC. Four major parameters must be taken in to account during this design process. The four parameters are the number of phases, the number of voltage levels, the switch configuration, and the DC input bus voltage ratio. The following chapter discusses advanced control algorithms necessary to improve the operation of the CMLC.

THIS PAGE INTENTIONALLY LEFT BLANK

III. CONTROL STRATEGIES FOR THE CASCADED MULTI-LEVEL CONVERTER

A. PURPOSE

This chapter discusses the differences between open-loop and closed-loop control. Additionally, this chapter provides a detailed description of the two most popular control strategies used to operate CMLCs.

B. OPEN-LOOP VERSUS CLOSED-LOOP CONTROL

Open-loop and closed-loop refer to the feedback path of the control system. For most applications closed-loop control is preferred. However, open-loop control is often implemented initially to test the design of a system.

1. Open-loop Control

An open-loop control system is controlled solely and directly by one or more input signals [7]. Figure 9 illustrates the basic concept behind an open-loop control system.

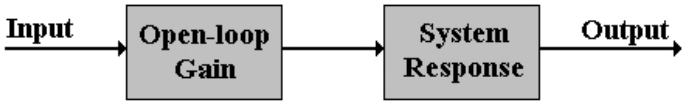

Figure 9. Open-loop Control System

As can be seen in Figure 9, there is no path from the output, back to the input. This means that the input of the system is completely independent of the output. Since the input is not affected by the output, there is no way to regulate the output to respond to changes in the system. For example, an open-loop motor controller would not be able to regulate a constant shaft speed for transient load operations. Therefore as the load changes, the shaft speed will either increase or decrease.

The inability of the open-loop controller to maintain a specific output condition for a given system is typically why open-loop controllers are not implemented in practice.

2. Closed-loop Control

A closed-loop control system is controlled by a combination of one or more input signals as well as one or more feedback signals [7]. Each system must be examined in order to determine the relevant input and feedback signals. Figure 10 illustrates the basic concept of a closed-loop control system.

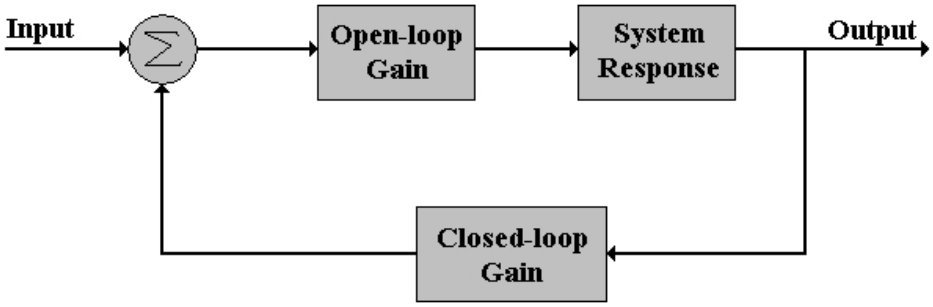

Figure 10. Closed-loop Control System

In Figure 10, the feedback path leads from the output, through a block representing the feedback gain, to the input. This feedback path provides a way for the output to affect the input. Now that the output of the system can influence the input to the system, the output can be regulated to account for changes in the system. For example, a closed-loop motor controller would be able to maintain a constant output speed regardless of how the load is changed. Depending on the feedback gain and other parameters, the output speed may change for a short amount of time; however, eventually the speed will return to its previous value.

When designed properly, closed-loop controllers add stability to a system, which an open-loop controller could never achieve. Additionally, closed-loop controllers allow engineers to design highly complex integrated systems.

C. SINE-TRIANGLE PULSE WIDTH MODULATION

PWM is the process of varying the duty cycle of a switch, or switches, while maintaining a constant switching frequency [11]. The duty cycle is simply the amount of time a switch is conducting versus the amount of time the switch is not conducting [11]. Sine-triangle PWM (SPWM) refers to the manner in which the PWM signal is generated.

For a 3/3 CMLC there are nine possible voltage levels that can be achieved by the converter. In order to determine which of the nine levels the converter should be producing, eight triangle waveforms are used as a basis for comparison with a reference sine wave. Figure 11 illustrates a SPWM system with eight triangle waves and a 60-Hz reference sine wave.

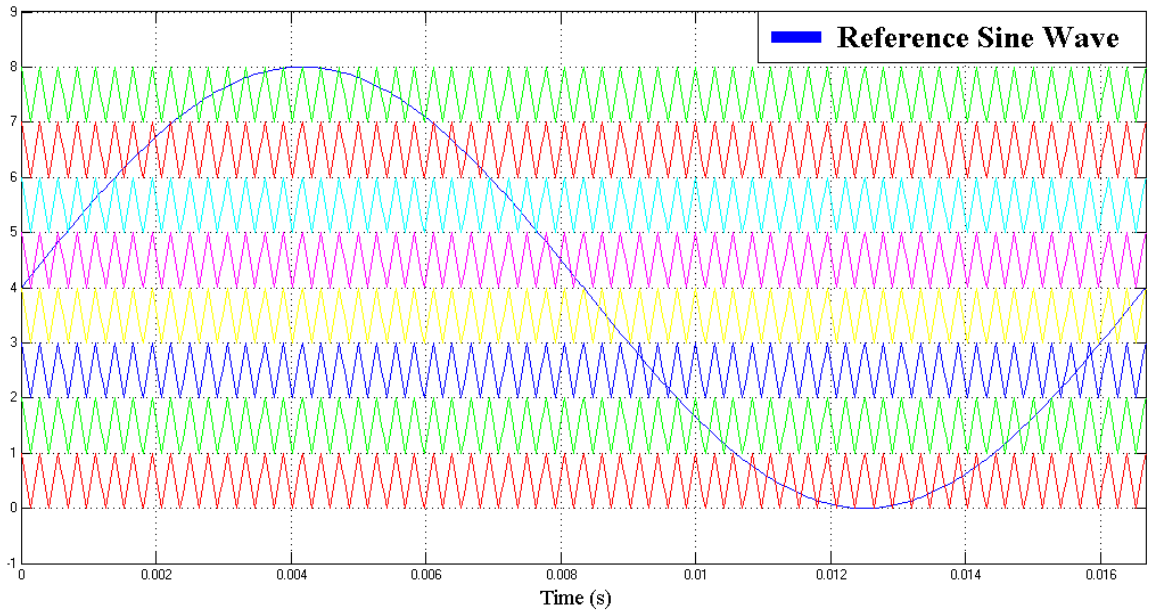

Figure 11. Nine Level SPWM System

The instantaneous value of the reference waveform is obtained at each sample point. This value is then compared to each triangle waveform to determine how many triangle waveforms the sampled value is greater than. The following example will clarify how the voltage level is obtained. From Figure 11, it can be seen that the instantaneous value of the reference sine wave at 4 ms is approximately 8. At this point the reference waveform has a larger magnitude than any triangle waveform; therefore the number of triangle waveforms the sample value is greater than is 8.

After making all the necessary comparisons a waveform similar to Figure 12 can be obtained.

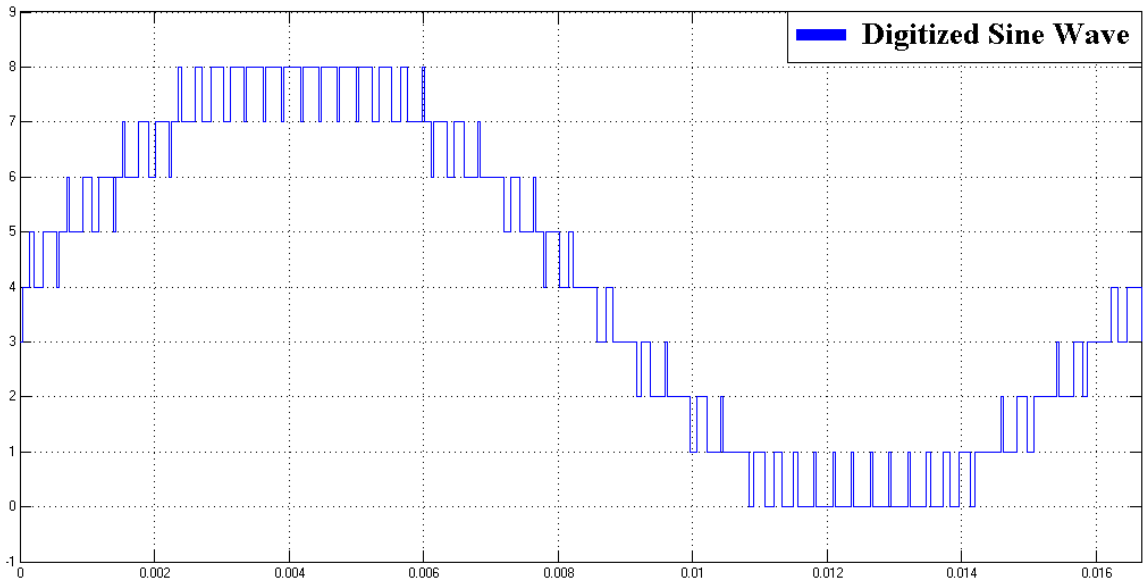

Figure 12. SPWM Voltage Level Output

The waveform in Figure 12 is essentially a digitized version of the reference sine wave. This process is very similar to the methods used to digitize voice signals in communications systems. Once the digitized waveform is created, the signal is sent to a switch decoder to determine which combination of switches will be needed in order to obtain the correct output voltage.

SPWM is a relatively simple way to produce a high fidelity output current from a given converter. However, SPWM has the significant drawback of being an open-loop control strategy. SPWM is considered mainly an open-loop control strategy because implementing a closed-loop control strategy would require the reference waveforms to change dynamically. To address this problem, a more complex algorithm known as Space Vector Modulation (SVM) has been developed.

D. SPACE VECTOR MODULATION

The basic principle behind SVM is to represent all possible voltage outputs of a converter in the *q-d* reference frame, which was previously discussed in Chapter II Section B. Equations 2.1, 2.2, and 2.3 are used to transform the phase voltages into the *q-d* reference frame. Figure 13 illustrates the voltage vector plot produced for a 3/3 CMLC where the input DC bus voltage ratio of the bulk to conditioning converter is 3:1.

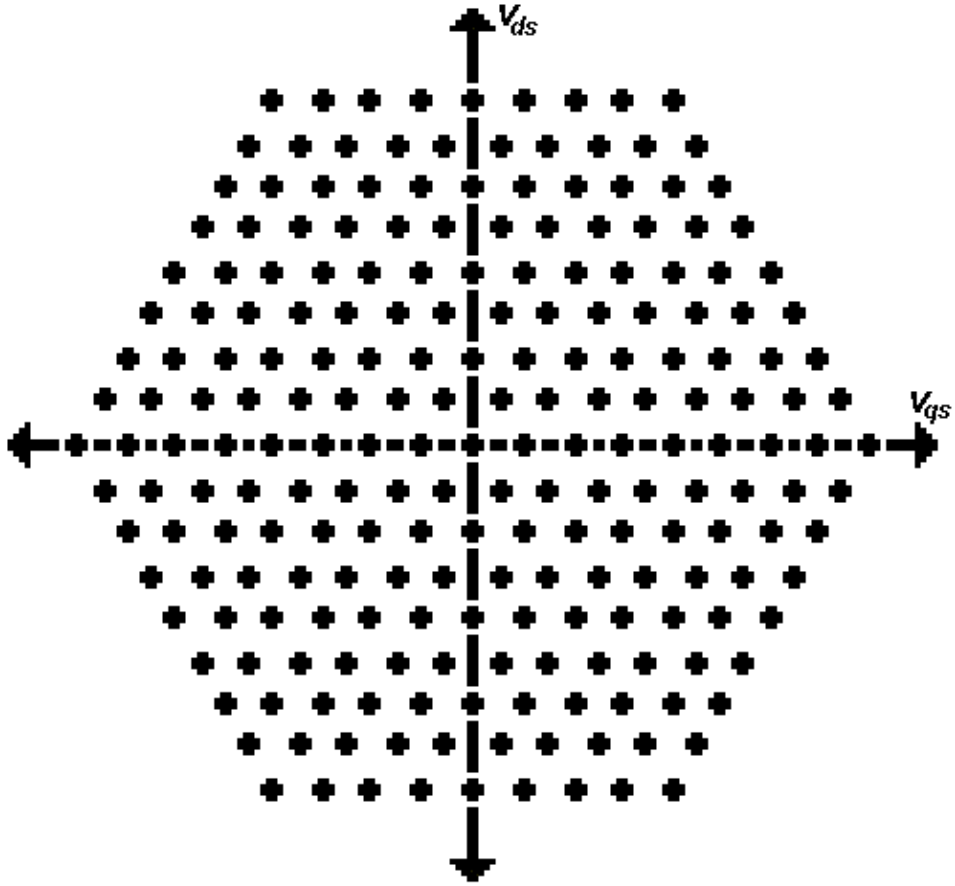

Figure 13. 3/3 CMLC Voltage Vector Plot

Each point on the plot in Figure 13 represents a specific state of the converter. A converter state consists of the position of all the switches for both the bulk and conditioning converters, as well as for all three phases. A sinusoidal voltage is created by rotating a reference voltage vector around the plot [11]. The result is a "ring" of switching states that will be used to approximate the voltage vector. Figure 14 illustrates the "ring" that is created by rotating the reference voltage vector around the plot.

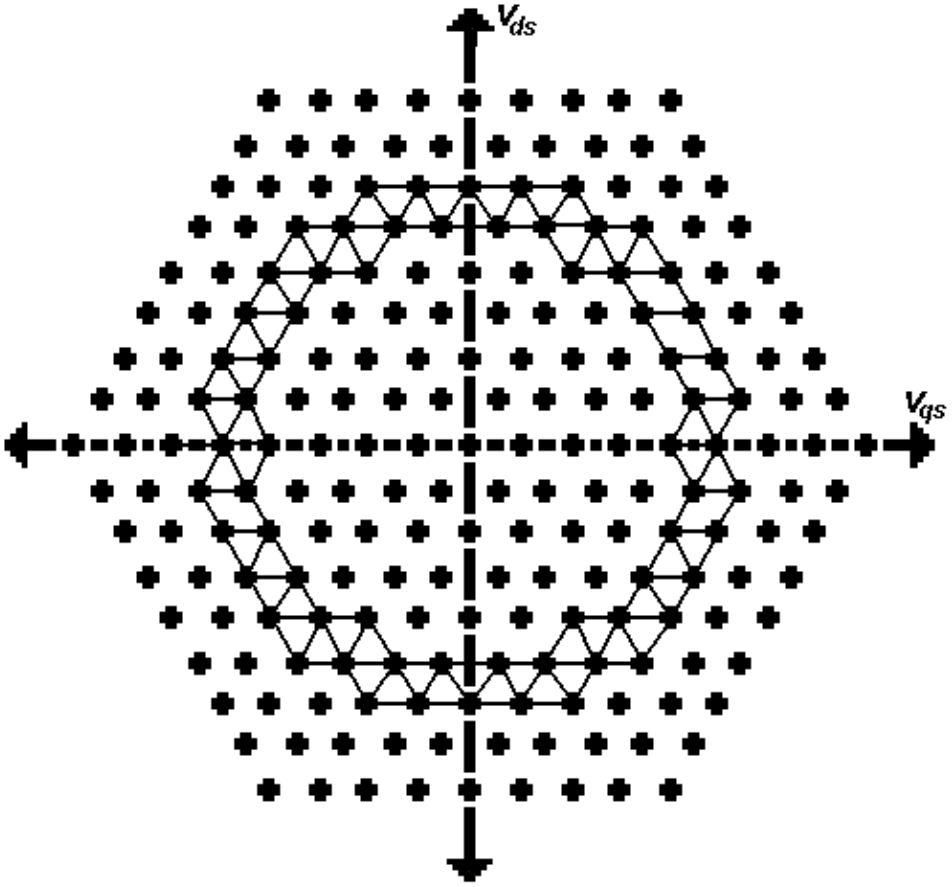

Figure 14. 3/3 CMLC Voltage Vector Plot with Reference Vector "Ring"

The reference voltage vector is approximated by selecting the three closest switching states of the converter [12]. Simple geometric relationships will determine the amount of time the converter should dwell in each state in order to accurately approximate the reference voltage vector. Once the algorithm determines the switching state of the converter, a simple table can be used to determine which switch combinations are required to produce the proper output voltage.

The main advantage of SVM over SPWM is that the reference voltage vector can be generated using a feedback loop, thus SVM can be made into a closed-loop control system [11]. Additionally, with careful analysis a switching pattern can be created to regulate the DC bus voltage of the conditioning converter using the positive power flow from the bulk converter [9]. This means that only one DC bus is required to power both the bulk and conditioning converters.

E. SUMMARY

Open-loop control systems are often implemented initially during prototyping due to their relatively simple design. Once the algorithm and hardware is tested, engineers often provide a feedback loop. This feedback loop is used to regulate a desired output. For example, a feedback loop for a motor could be used to provide a constant output speed, regardless of the load conditions. There are two algorithms most commonly used to control a CMLC, SPWM and SVM. SPWM is a relatively simple algorithm that gives a desirable output current waveform. However, due to the fact that SPWM is an open-loop control strategy it is often only used in initial design prototyping. SVM is the closed-loop solution for control of a CMLC. Due to the ease of implementation, the SPWM control strategy was used as the basis of this thesis. The following chapter discusses the implementation of the SPWM control strategy.

THIS PAGE INTENTIONALLY LEFT BLANK

IV. IMPLEMENTATION OF CONTROL STRATEGY

A. PURPOSE

The purpose of this chapter is to discuss the specific details of implementing the strategy used to control the 3/3 CMLC constructed at NPS. The algorithm was developed using a simulation software package. Once the algorithm was tested, it was compiled onto a Digital Signal Processor (DSP) board and routed to the hardware.

B. SIMULATION SOFTWARE

The simulation software package used for the development and testing of the controller for the 3/3 CMLC constructed at NPS is Matlab Simulink. Simulink allows users to quickly and easily create a variety of different control systems for development and testing purposes.

The controller design that was chosen for development is the SPWM. Figure 15 illustrates the top-level view of the SPWM controller in Simulink.

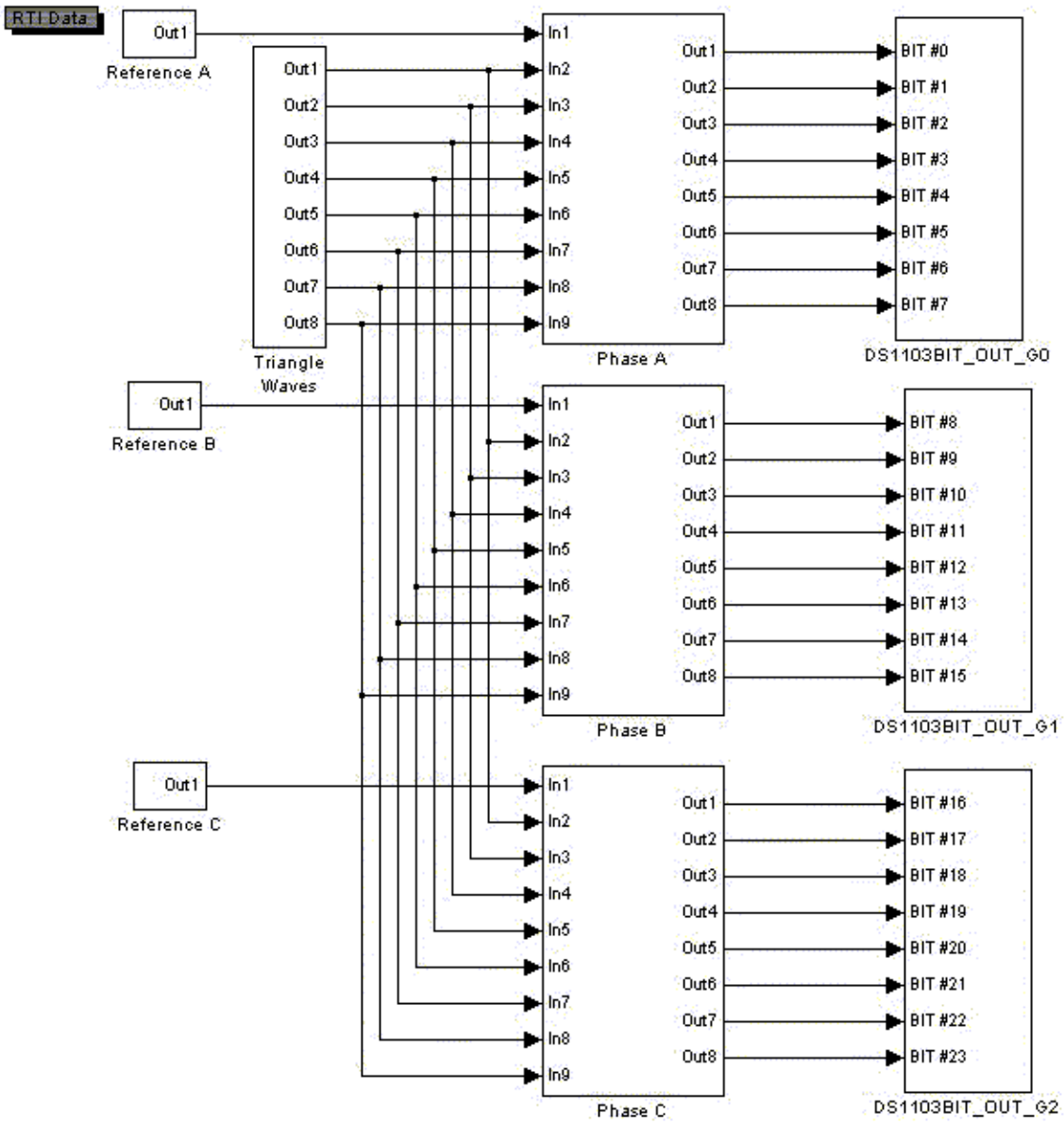

Figure 15. Simulink Model of SPWM Controller

The controller in Figure 15 consists of three reference signals, a set of triangle waveforms, three phase-legs, and three DSP interface ports.

1. Reference Signal Generator

The three reference signal generators in Figure 15 are labeled *Reference A*, *Reference B*, and *Reference C*. The reference signal generators are identical except that the generated signals are 120˚ out-of-phase with each other. The Simulink reference signal

generator can be expanded to show the internal components. Figure 16 shows the expanded view for phase "A."

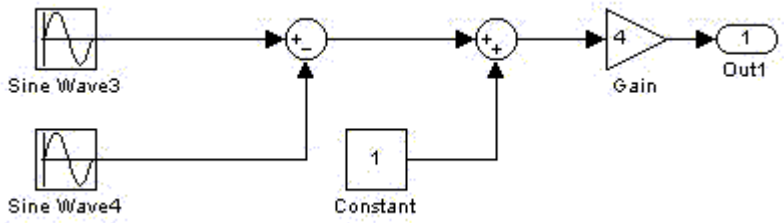

Figure 16. Reference Signal Generator (Phase A)

The SPWM reference signal chosen for this converter is slightly different than previously discussed. Instead of using a sine wave as the reference signal, the following signal is used:

$$r(t) = 4\left[1 + \cos(2\pi 60) - \frac{1}{6}\cos\left(2\pi\left(3(60)\right)\right)\right]. \qquad (4.1)$$

Equation 4.1 describes a sine wave with a DC offset and third harmonic injection. The DC offset is added to make indexing into the switch decoder table easier. (The switch decoder table will be discussed later in this chapter.) Third-harmonic injection is used to boost the power output of the converter by taking advantage of the balanced three-phase load [13]. Since all triplen harmonics are eliminated in a three-phase wye-connected floating-neutral point system, the power output can be raised by adding these harmonics to the reference signal [13]. In this case only the third harmonic is added for simplicity. Figure 17 illustrates the output of the reference signal generator for phase "A."

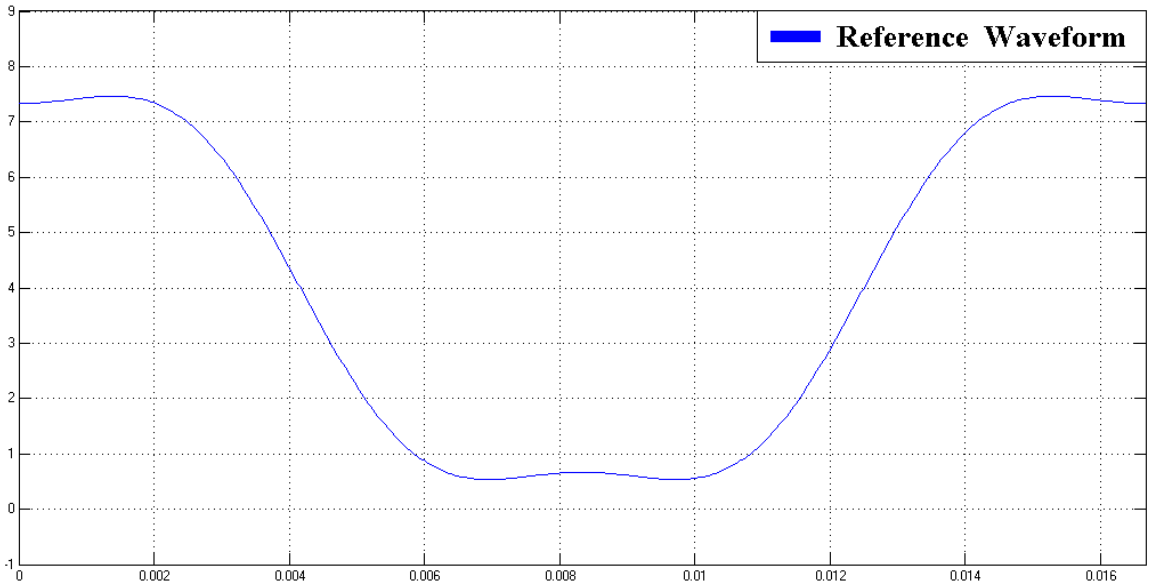

Figure 17. Phase A Reference Signal

As can be see in Figure 17, the signal is essentially a flattened sine wave. The reference signals for phase "B" and phase "C" are similar to that shown in Figure 17, the only difference being the 120˚ phase shifts.

2. Triangle Waveform Generator

Since all three phases require the same set of triangle waveforms, only one triangle waveform generator is needed. This block is labeled *Triangle Waves* in Figure 15. The triangle waveform generator consists of eight Simulink repeating sequence blocks. For each repeating sequence there are two matrix parameters required. The first parameter is the time values for the sequence. The second parameter is the output values that correspond to the time values. For example, a triangle waveform that has an upper bound of 1, a lower bound of 0, and a frequency of 10 Hz would have the following matrix parameters: [0 0.05 0.1] and [0 1 0].

The triangle waveform frequency determines the overall switching frequency of the converter. For this thesis, a switching frequency of 3600 Hz was used. The output of the triangle waveform generator and the reference signal generator make up the inputs to the phase-leg. These input signals can be seen in Figure 18 for phase "A."

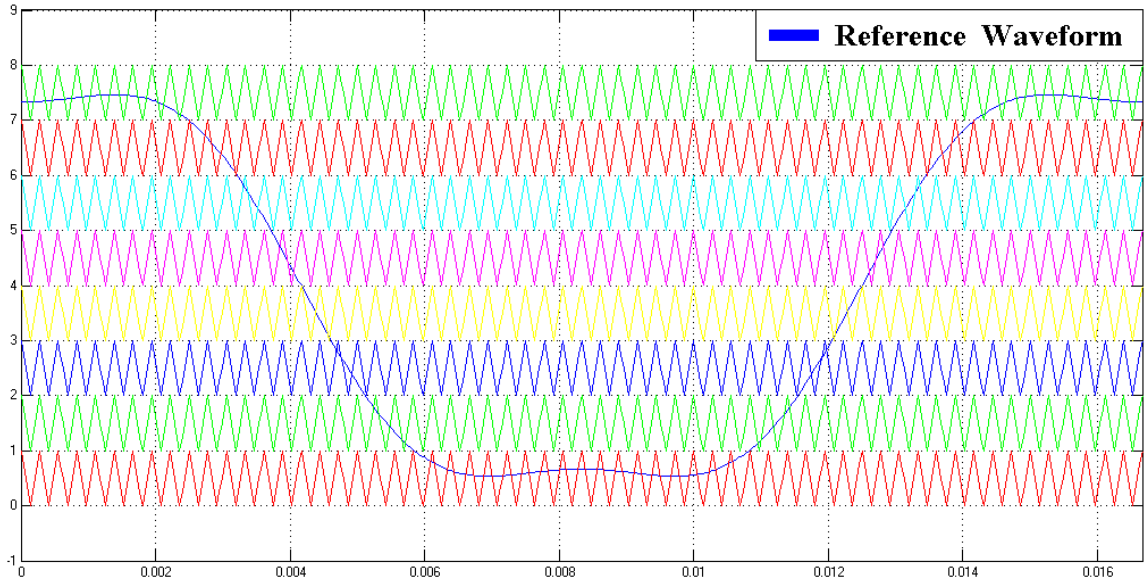

Figure 18. Phase-Leg A Input Signals

The eight triangle waveforms are clearly visible in Figure 18. These eight waveforms in addition to the reference signal will be used to create the PWM signal that is fed to the switch decoder table.

3. Phase Leg

The three phase-legs located in Figure 15 are labeled *Phase A, Phase B,* and *Phase C.* All three phase-legs are constructed identically. The purpose of the phase-leg is to generate the gating signals required to fire the switches in the 3/3 CMLC. Figure 19 is an expanded view of the phase-leg for phase "A."

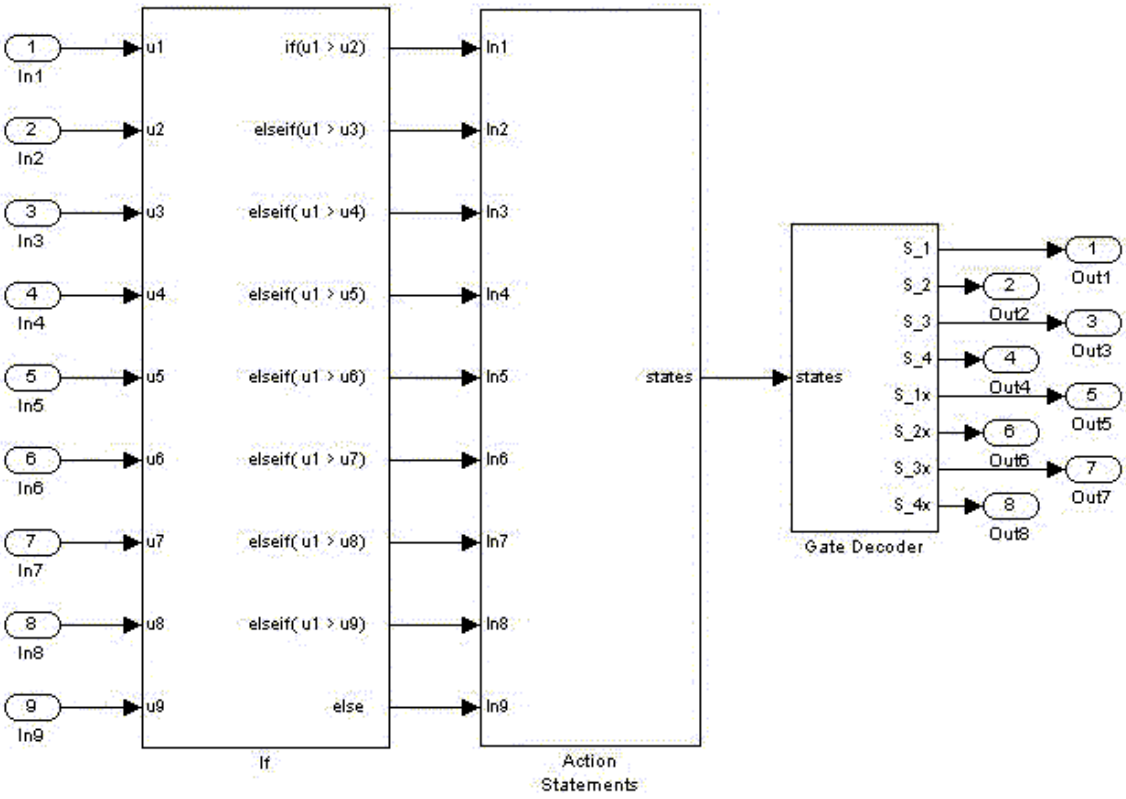

Figure 19. Phase-Leg A Expanded View

The phase-leg consists of three basic components. The first block, labeled *If*, compares the reference signal with the eight triangle waveforms. Each triangle waveform has an upper bound and a lower bound. This block is used to determine which triangle wave's upper and lower bounds encompass the sampled reference signal value. Once this triangle waveform is identified, a state (number from zero to eight) is assigned using the *Action Statements* block. The output labeled *states* is essentially a digitized representation of the original reference signal. Figure 20 shows the output labeled *states* superimposed over the original reference signal.

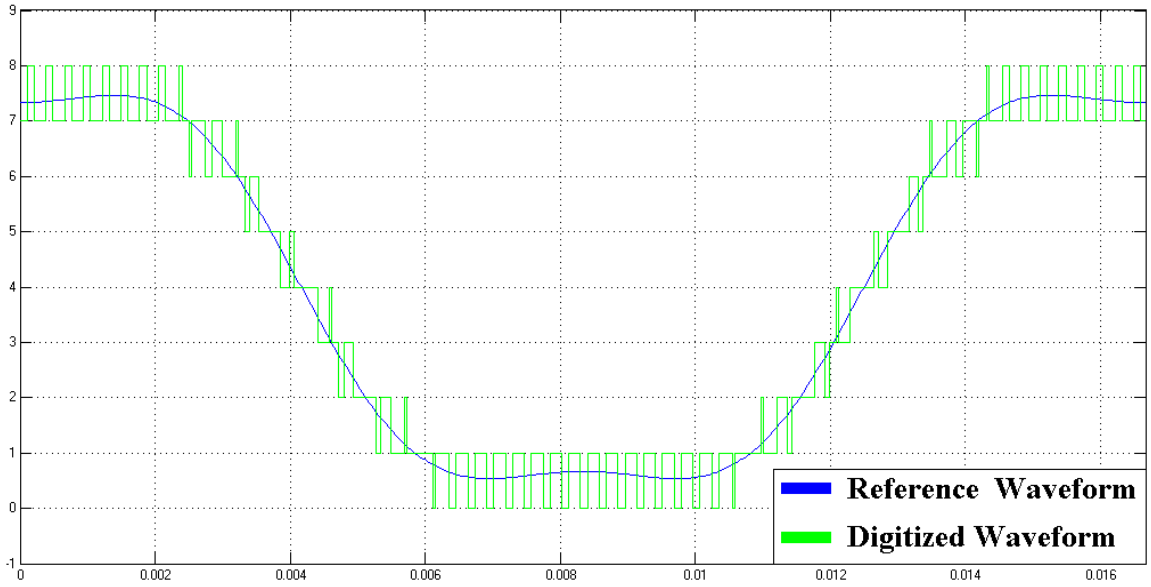

Figure 20. Digitized Reference Signal

The digitized reference waveform (green) can be seen in Figure 20. The original reference signal (blue) is superimposed over the digitized signal in order to illustrate the relationship between the two signals. At this point it should be obvious to see that if the number of states, or voltage levels, were increased; the digitized waveform would more closely approximate the reference signal. Additionally, the reference signal could be better approximated by an increase in the switching frequency, which is simply the frequency of the triangle waveforms.

Now that the reference signal has been digitized, it can be sent into the switch decoder table, labeled *Gate Decoder* in Figure 19. The switch decoder table is simply a module that determines which switches need to be fired in order to create the desired state (output voltage level). Figure 21 shows the expanded view of the *Gate Decoder*.

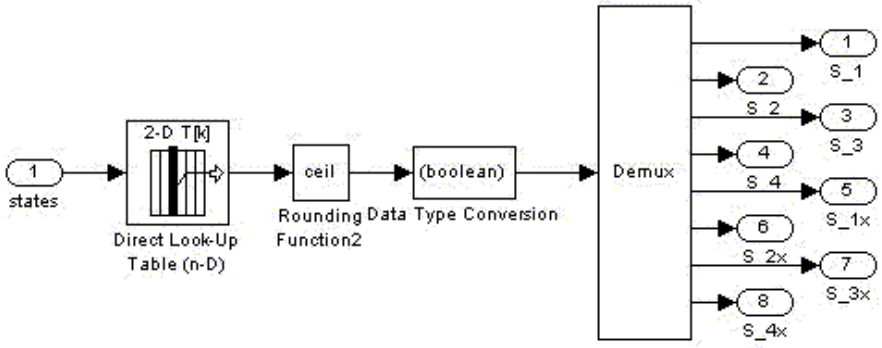

Figure 21. Gate Decoder Expanded View

The key block in Figure 21 is the *Direct Look-Up Table*. This look-up table is where the gating signals are stored for each switch on the 3/3 CMLC. Without this table, the controller would not know what switches must be fired in order to create the desired output voltage based on the reference signal. Table 2 displays the data that is stored in the look-up table.

State	S1	S2	S3	S4	S1x	S2x	S3x	S4x
0	0	0	1	1	1	1	0	0
1	0	0	1	1	0	1	1	0
2	0	0	1	1	0	0	1	1
3	0	1	1	0	1	1	0	0
4	0	1	1	0	0	1	1	0
5	0	1	1	0	0	0	1	1
6	1	1	0	0	1	1	0	0
7	1	1	0	0	0	1	1	0
8	1	1	0	0	0	0	1	1

Table 2. Gate Decoder Look-Up Table

The *Gate Decoder* is fed with the state signal from Figure 20 (green curve). The output of the table is the contents of the entire row that corresponds to the state. For example, if the value of the state signal is 4, then the output of the table is the following matrix: [0 1 1 0 0 1 1 0].

The ceiling function is then used to ensure sharp transitions between the output signals when the state changes. This block was added after experimentation showed that these transitions sometimes ramped instead of being a perfect step transition. The *Data Type Conversion* block in Figure 21 converts the table output values into Boolean logic values which are required by the DSP interface ports. Finally, the *Demux* block is simply a demultiplexer which converts the matrix output of the table into eight separate gating signals.

Figure 22 shows the switching sequence for all eight switches during one reference signal period.

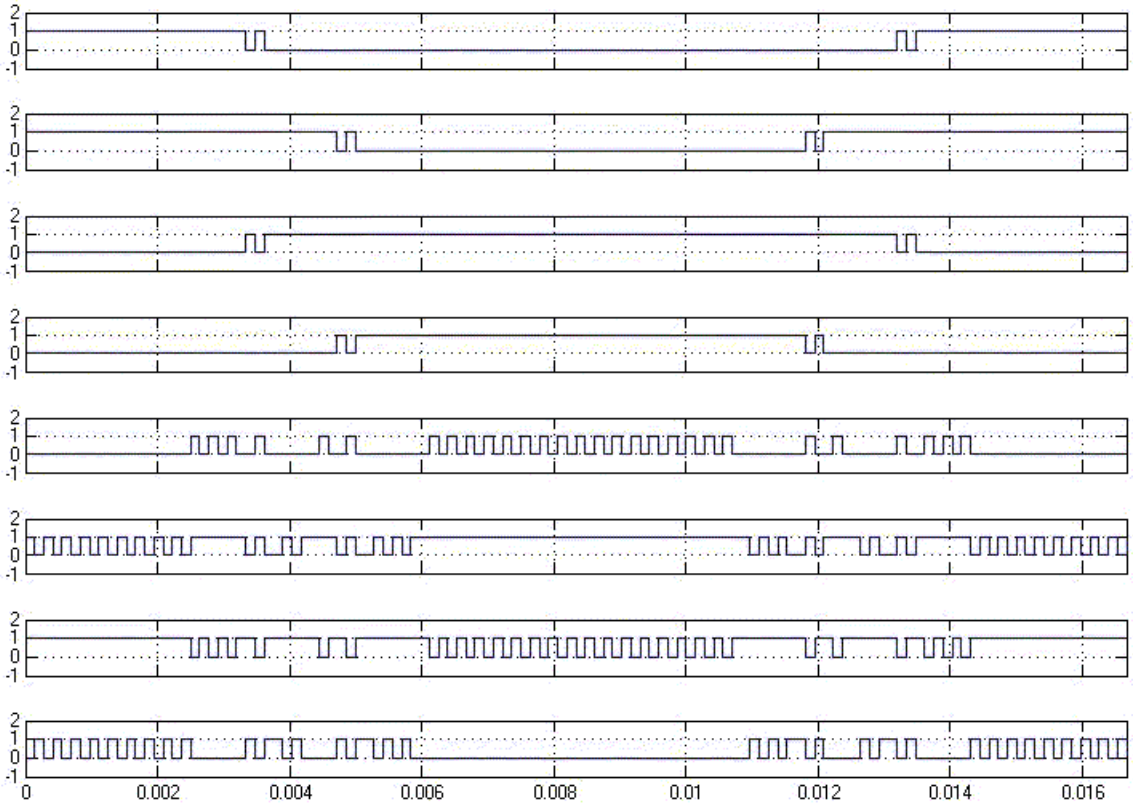

Figure 22. Switching Sequence for Eight Switch Phase-Leg over one Reference Signal Period

The top four plots in Figure 22 represent the four switches associated with the bulk converter (S1–S4). The bottom four plots in Figure 22 represent the four switches associated with the conditioning converter (S1x–S4x). A "1" represents that a switch is conducting where as a "0" represents that a switch is not conducting. It is interesting to note that the bulk converter switches transition much less frequently then those of the conditioning converter.

4. DSP Interface Port

The DSP interface port allows the DSP card to connect the actual converter hardware with the software controller. Three DSP interface ports can provide 24 different digital I/O lines. Section C in this chapter will cover the DSP interface in more detail.

C. DIGITAL SIGNAL PROCESSOR INTERFACE

The DSP interface chosen for this thesis was the DS1103 module produced by dSPACE. The goal of dSPACE is to provide a transparent interface for Rapid Control Prototyping (RCP) and Hardware-In-the-Loop (HIL) simulation. The basic concept behind RCP is to allow new control designs to be implemented and tested on real-time hardware without the need of building full production hardware [14]. With the use of RCP, control algorithms can be refined quickly and easily. Once testing is completed on the algorithm, the production hardware can be produced with confidence in its performance.

Additionally, academic and research institutions benefit from the RCP concept. Once the initial investment is made to purchase the dSPACE hardware and software, very little money needs to be spent to make numerous control designs. dSPACE has eliminated the need to send off controller designs to expensive and time-consuming prototyping facilities.

Prototyping a design is a quick and easy way to develop a robust control algorithm. However, in order to refine the control design, all of the hardware components need to be simulated. Since this is often not the most practical solution, dSPACE has developed HIL simulation. HIL simulation essentially means that some actual hardware will be connected to the simulation through the DSP interface [14]. This connection allows for design and testing on actual hardware components, instead of testing in a purely computer simulated environment.

With the use of RCP and HIL simulation, complex designs can be implemented quickly and cost effectively. The dSPACE interface consists of three main components: the DSP card, the DSP I/O board, and the DSP software interface, which will be discussed in the following section.

1. DSP Card

The DS1103 Power PC (PPC) controller board is a single-board system and is shown in Figure 23. The board is inserted into a standard Peripheral Component Interconnect (PCI) card slot of a computer tower.

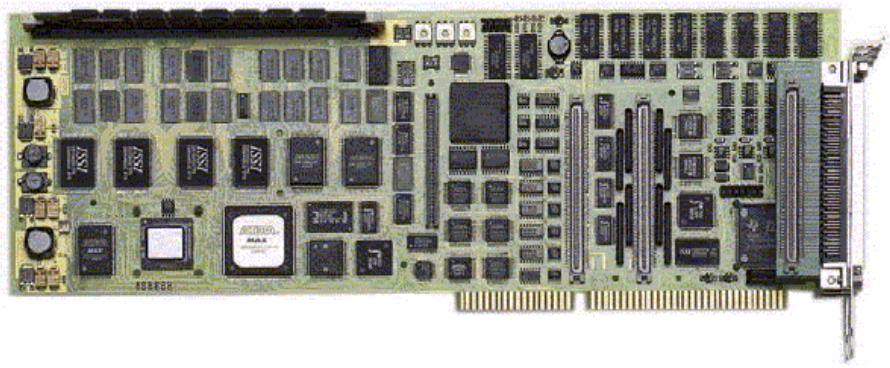

Figure 23. DS1103 PPC Controller Board [From Ref. 15.]

The DS1103 card shown in Figure 23 is designed to meet all the requirements of a complex DSP design. The card contains all the necessary components for the processor and I/O.

2. DSP I/O Board

The CP1103 I/O board was chosen to interface the hardware with the DSP card and is shown in Figure 24.

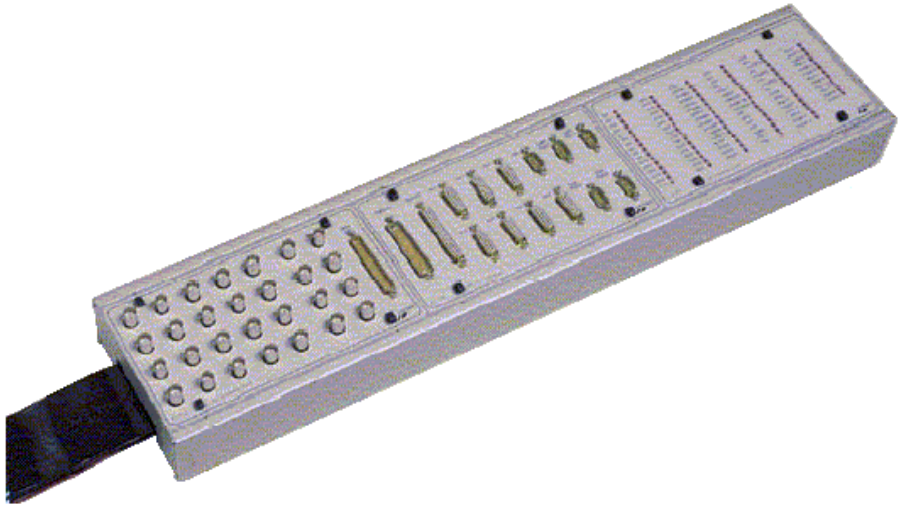

Figure 24. CP1103 I/O Board [From Ref. 16.]

As can be seen from Figure 24, the CP1103 contains numerous input and output ports. The interface port that was used to connect the DSP card to the 3/3 CMLC at NPS was the 50-pin digital I/O connector. The pin configuration diagram can be found in Appendix A.

3. DSP Software Interface

The DSP software can essentially be divided up into two components. The first component is the Simulink interface. Simulink uses a modular design. In order to maintain the same functionality, dSPACE designed interface port modules for use in Simulink. These modules allow the standard Simulink blocks to interface with the hardware. Additionally, a real-time compiler was added to Simulink in order to load the DSP card with the desired simulation.

The second component is the *Control Desk* interface. This software takes the compiled code from Simulink and loads it onto the DSP card. Once the DSP card has been loaded, the simulation can be run in real time with HIL. Additionally, the *Control Desk* program allows the user to view all the signals going into and out of the DSP card as well as change parameters in the simulation.

D. SUMMARY

Once the controller is designed in Simulink, the algorithm can be compiled onto the dSPACE card. The card then sends the necessary control signals to any hardware. With the combination of dSPACE and Simulink, control algorithms can be designed and tested on real hardware quickly and cost effectively. The next chapter will discuss the design, testing, and performance of the 3/3 CMLC at NPS operated using the Simulink and dSPACE control interface.

V. HARDWARE PERFORMANCE ANALYSIS

A. PURPOSE

This chapter provides a detailed description of the 3/3 CMLC constructed at NPS. Additionally, this chapter discusses the tests performed on the converter as well as an analysis of the results obtained.

B. CONSTRUCTION OF THE CASCADED MULTI-LEVEL CONVERTER

The 3/3 CMLC constructed at NPS was built by Robert Crowe. Crowe's thesis, *Design, Construction and Testing of a Reduced-Scale Cascaded Multi-Level Converter*, provides a detailed description of the design and construction process [17]. This section will focus on the changes made to the original design.

The most noticeable change to the design is the new layout of the converter. The converter layout was changed in order to match the schematic in Figure 7. In the process of changing the layout, copper bus bars were created to connect all the switches to each other and also to the DC busses. This change in design will allow higher voltages and currents to be fed through the converter. Figure 25 illustrates the layout of the 3/3 CMLC with the new copper bus bars.

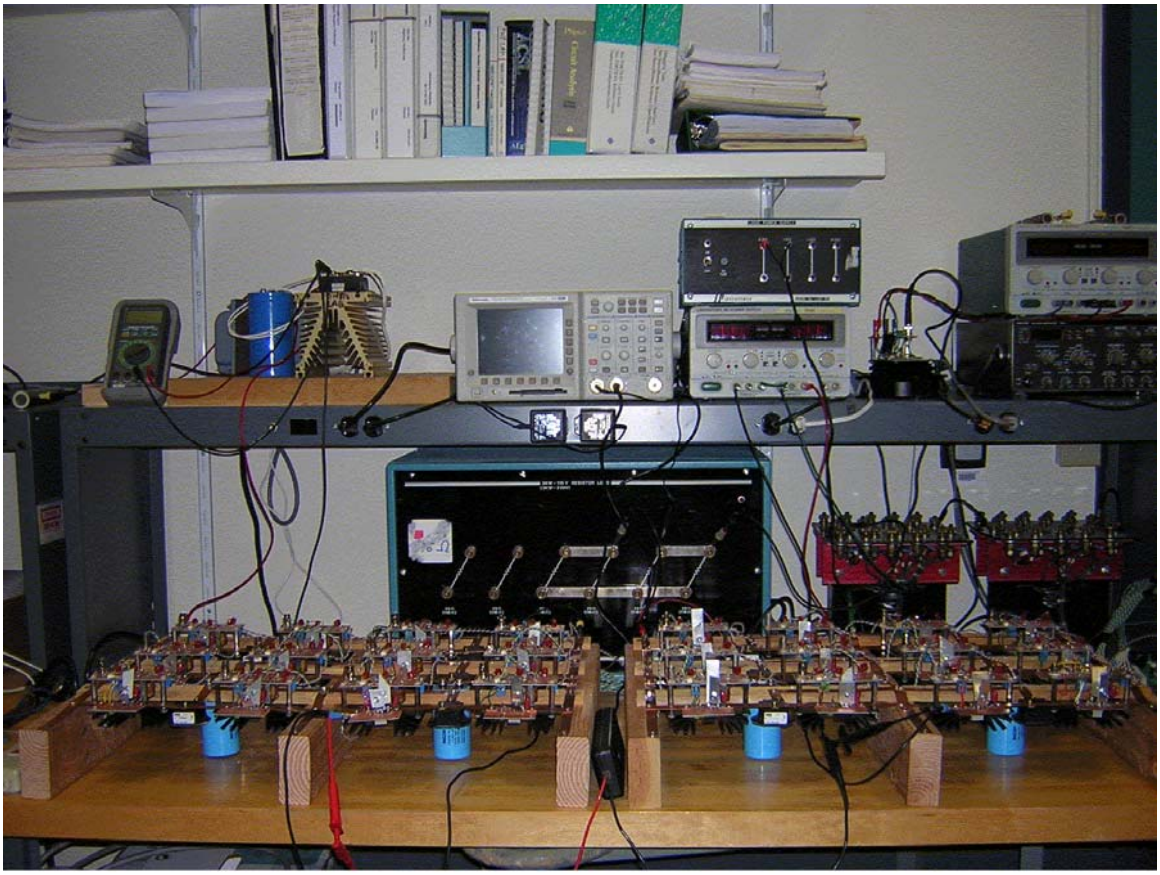

Figure 25. 3/3 CMLC Construction

The converter consists of two identically constructed multi-level converters. The converter on the left of Figure 25 was operated as the bulk converter; where as the one on the right was operated as the conditioning converter. Figure 26 provides a close-up view of the individual converter construction.

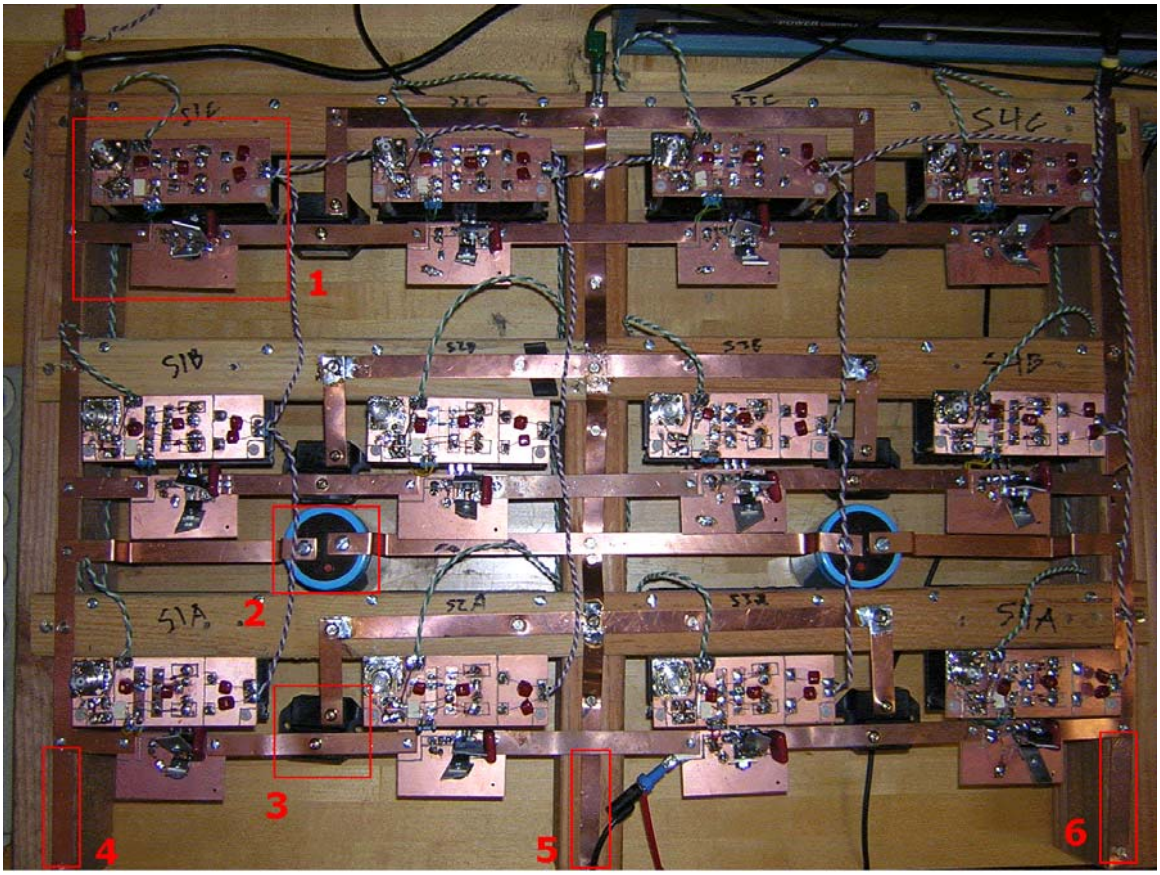

Figure 26. Close-up View of the Bulk Converter

As can be seen in Figure 26, each converter consists of twelve switching modules (one module is highlighted and labeled “1”), two capacitors (labeled “2”), six diodes (labeled “3”), two DC bus bars (labeled 4 and 6), and the neutral point bus bar (labeled 5). The two capacitors are used to regulate the voltage on the DC bus and reduce voltage ripple. The six diodes are used to neutral-point clamp the switches as discussed in Chapter II Section B. The DC input bus bars are used to provide power to the converter. Finally, the switch modules are used to create the AC output of the converter.

The switch modules are the most complicated portion of the whole converter. Each module consists of three main sections: the snubber card, the gate driver card, and the IGBT switch. The snubber card and IGBT switch remained unmodified. However, two design changes were made to the gate driver card.

The purpose of the gate driver is to provide a floating ground for each switch [17]. The gate driver consists of two inputs and one output. Figure 27 shows the original schematic diagram of the gate driver card.

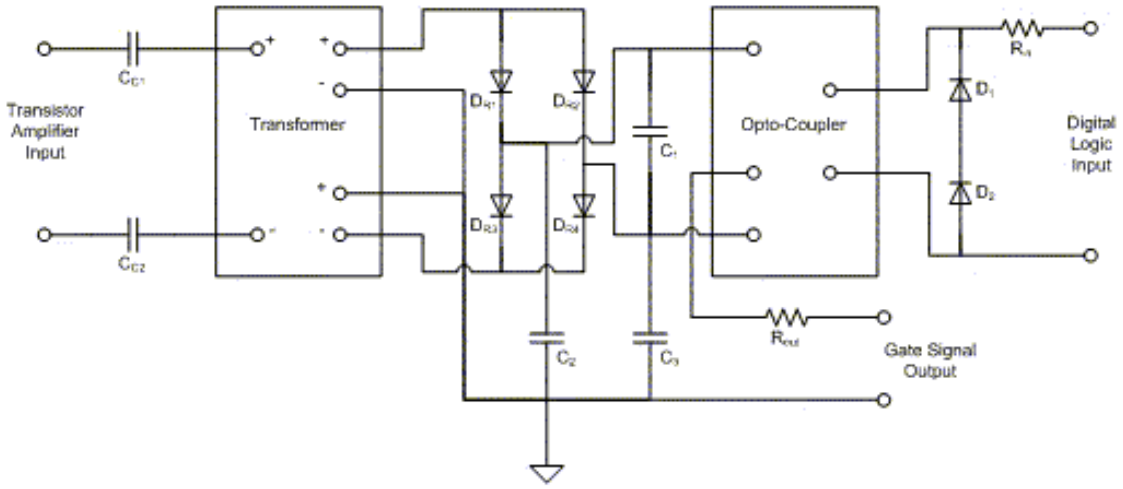

Figure 27. Original Gate Driver Schematic Diagram [After Ref. 17.]

The inputs and outputs of the gate driver are visible on the schematic in Figure 27. The first input, labeled *Transistor Amplifier Input*, provides a 20-kHz square wave to the primary side of a pulse transformer. The pulse transformer is used to isolate the gate driver from the power supply. The secondary of the pulse transformer is connected to a full-wave diode rectifier. The input square wave amplitude is adjusted to provide $\pm 15\ V_{DC}$ at the output of the rectifier. This $\pm 15\ V_{DC}$ is used to power the *Opto-Coupler*.

The second input to the gate driver card is labeled *Digital Logic Input*. This input is provided by the DSP card. The logic signal is simply the gating signal developed by the SPWM controller. This input is fed directly to the opto-coupler. The opto-coupler is used to isolate the gate driver's ground from the ground of the DSP card. Originally, the digital logic input to the gate driver card was provided through a coaxial cable that connected to a BNC connector mounted on the gate driver card. In order to interface with the DSP I/O board, this connection was replaced by a two-wire terminal connector. A twisted-pair wire was then used to connect the DSP I/O board to the terminal connection. All twenty-four switches had to be modified before the converter was ready for testing.

The output of the gate driver is the gate signal, labeled *Gate Signal Output*. The gate signal is an amplified and isolated copy of the digital logic input signal. The output signal feeds directly into the gate of the IGBT switch. During testing it was discovered that the IGBTs would turn on faster than they could turn off. This condition caused the positive and negative voltage rails to be shorted to the neutral point for a brief period of time. There are two possible solutions to this problem. In order to prevent two switches from conducting at the same time, either the turn-on time of the switches can be increased or a delay, known as blanking time, can be inserted. The following sections will discuss these two options.

1. Turn-on Time Increase

The goal of this method is to increase the amount of time it takes the switch to turn on, while leaving the turn-off time unchanged. When the turn-on time of a switch is increased, the switch is essentially slowed down. The turn-on and turn-off speed of a switch is dictated by the following equation:

$$\tau = RC\,, \tag{5.1}$$

where τ is the time constant for the switch, R is the resistance in the discharge path of the switch's capacitance, and C is the value of the capacitance in the circuit. If the value of τ is increased, then the switch will take a longer amount of time to turn on or turn off. If the value of τ is decreased, then the switch will take a shorter amount of time to turn on or turn off [18].

The value of this time constant for the circuit shown in Figure 27 depends on R_{out} and the capacitance of the gate-to-emitter junction in the IGBT. Since it was discovered that the turn-on time was too fast, the time constant for the turn-on circuit must be increased. Figure 28 shows the modified circuit used to create this turn-on time increase.

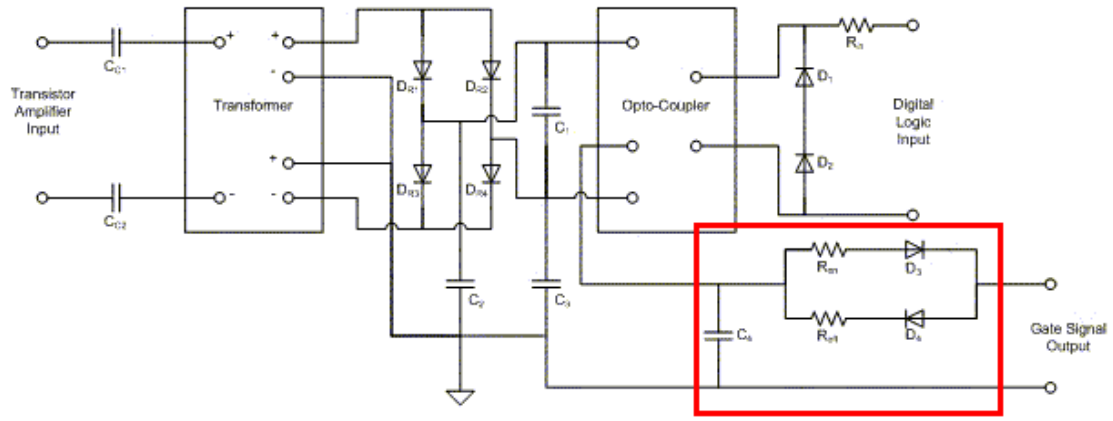

Figure 28. Modified Gate Driver Schematic Diagram

Figure 28 highlights the additional circuitry that was added to the gate driver card. The additional circuitry consists of two resistors, two diodes, and a capacitor. When the gate is being turned on and turned off, the value of the time constants are given by the following equations:

$$\tau_{on} = R_{on}\left(C_4 + C_{GE}\right) \tag{5.2}$$

and

$$\tau_{off} = R_{off}\left(C_4 + C_{GE}\right). \tag{5.3}$$

If the goal is to increase the turn-on time, then the value of R_{on} in Equation 5.2 needs to be significantly larger than the value of R_{off} in Equation 5.3. This method was implemented in the lab because of time constraints; however, adding blanking time would be a better solution as discussed below.

2. Blanking Time

Instead of changing the rate at which the switch is capable of turning on, the blanking time method inserts a brief delay into every switching period. This delay has to be long enough to ensure that all the switches are off before the start of the next switching period. Since every switch in the converter receives this delay, the output of the converter will be unchanged. Figure 29 shows the necessary additions needed to implement blanking time for the gate driver card.

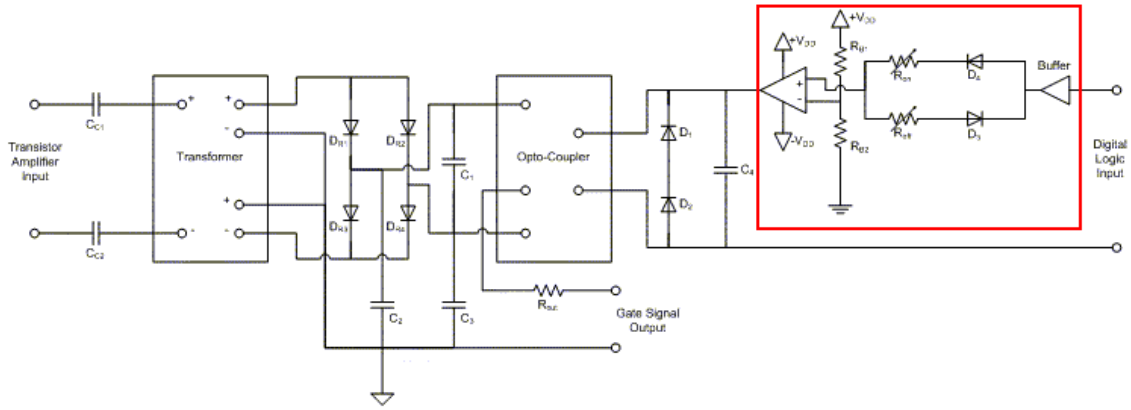

Figure 29. Proposed Gate Driver Schematic Diagram

As can be seen in Figure 29, two variable resistors, two resistors, two diodes, an operational amplifier, a buffer, and a capacitor are added to the circuit. This circuit operates similarly to the one discussed in the previous section; however, since the circuit is not connected to the gate of the IGBT, the switching speed of the IGBT is unaffected. This circuit simply adds a delay to the digital logic input signal. This delay causes a brief logic value of zero to be sent to the gates of all the switches in the converter at the beginning of every switching period. Variable resistors were chosen for this application in order to tune the value of the logic delay. This delay should be made as small as possible for each switch. Additionally, a buffer is added to the output of the dSPACE I/O board to ensure that the logic signal is powerful enough to drive the new delay circuit. Finally, an operational amplifier is used as a comparator to meet the opto-coupler's manufacturer input slope requirement. Implementing the gate driver circuit in Figure 29 would be relevant material for a follow-on thesis.

Once the digital logic input terminals and the turn-on time increase circuit were added to the gate driver card, testing of the SPWM control algorithm was started.

C. TESTING OF THE CASCADED MULTI-LEVEL CONVERTER

Testing of the 3/3 CMLC and SPWM control algorithm was conducting in three distinct stages. The three stages of testing were initial DSP testing, single-phase testing of the 3/3 CMLC, and three-phase testing of the 3/3 CMLC. The following sections will discuss these three stages of testing.

1. Initial DSP Testing

Initial DSP testing was conducted in order to figure out how to integrate the Simulink code, DSP software and hardware, and the actual hardware in the lab. The first test performed used a Simulink function generator module to send a signal to the digital I/O port. This signal was confirmed using an oscilloscope. Once the presence of the signal was confirmed, the gate of an IGBT was connected to the digital I/O port. The oscilloscope was then used again to confirm that the IGBT was being fired properly. The purpose of the initial testing was mainly to ensure that the DSP interface was setup correctly. More extensive testing of the converter and controller were conducted during the second stage.

2. Single-Phase Testing

Of the three phases of testing, the single-phase tests were the most extensive and time consuming. Each phase-leg was connected to a $58\ \Omega$ resistor and a 42.5 mH inductor. The three phase-legs of the converter were then tested independently to ensure proper operation. Many minor problems were corrected. These problems usually consisted of replacing damaged or missing components. One major problem encountered was the shorting of the DC busses due to improper switching. This problem was resolved by modifying the gate driver card as previously discussed.

Additionally, during the initial single-phase testing it was found that in order to develop an output across the load, the neutral points of the bulk and conditioning converters needed to be connected. This connection was later removed when three-phase testing was conducted. Once proper operation was confirmed on the three phases operating independently, three-phase testing was conducted.

3. Three-Phase Testing

Since the converter was designed to power a three-phase resistive-inductive load, this was the most interesting set of tests conducted. Three-phase testing was conducting using incremental DC bus voltages. Table 3 lists the voltage increments used during testing.

Test	V_{dc}	V_{dcx}
1	30	10
2	60	20
3	90	30
4	180	60
5	270	90

Table 3. Bulk and Conditioning Converter DC Bus Voltages

As can be seen in Table 3, the DC bus voltages (V_{dc} and V_{dcx}) started low and were raised incrementally until the load was being operated at its rated power. Tests one through three were conducted using three $58\ \Omega$ resistors and three 42.5 mH inductors placed in series. Eventually the inductive load was reduced to 4.25 mH. Tests four and five were conducted using a quarter horsepower three-phase induction motor. Since the goal of this thesis was to test the operation of the converter while powering a three-phase motor, all the results were taken while the motor was being operated at rated power. The following section explains the results obtained during the final three-phase test.

D. PERFORMANCE ANALYSIS

Performance analysis was conducted using a quarter horsepower three-phase induction motor operated at rated power. This section provides a detailed analysis of the converter's performance under rated load conditions.

Figure 30 illustrates the motor load setup used to test the 3/3 CMLC in the lab for the final performance analysis.

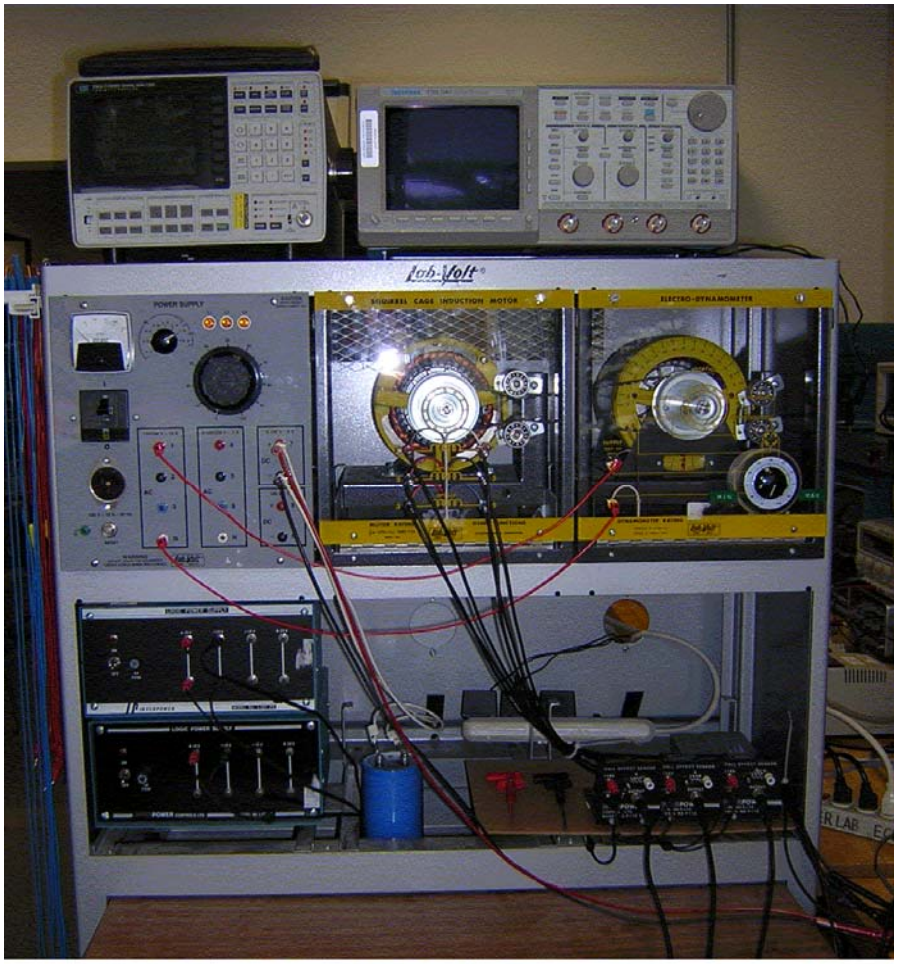

Figure 30. Motor Load Setup

In addition to the motor itself, Figure 30 illustrates the other equipment required to perform the test. This equipment included a spectrum analyzer, four-channel oscilloscope, dynamometer (with power supply), and three Hall-Effect current probes (with power supplies).

The spectrum analyzer was used to measure the harmonic content of the phase current. Additionally, the Total Harmonic Distortion (THD) of the phase current can be measured using the spectrum analyzer. This measurement is dictated by the following equation:

$$\%\text{THD} = 100\sqrt{\sum_{h\neq 1}\left(\frac{I_{s,h}}{I_{s,1}}\right)^2}\ , \tag{5.4}$$

where $I_{s,h}$ refers to the magnitude of the h^{th} current harmonic and $I_{s,1}$ refers to the magnitude of the fundamental current [7]. The spectrum analyzer used in this thesis was capable of measuring the first twenty harmonics to produce the THD.

The oscilloscope was used to graphically display the voltage and current waveforms. Also, the oscilloscope was used to measure waveform parameters such as peak amplitude, frequency, and phase angle. The dynamometer was used to provide the torque required to operate the induction motor at rated conditions. Finally, the Hall-Effect current probes were used to measure the three phase currents.

The final performance analysis consisted of two separate stages of testing. The following sections will discuss the phases of testing as well as the results obtained in each stage.

1. Bulk Converter Testing

The first stage of testing consisted of operating the 3/3 CMLC as a single multilevel converter. This operation means that the bulk converter input DC bus was powered, while the conditioning converter remained without power. Figures 31 and 32 illustrate the results of this test.

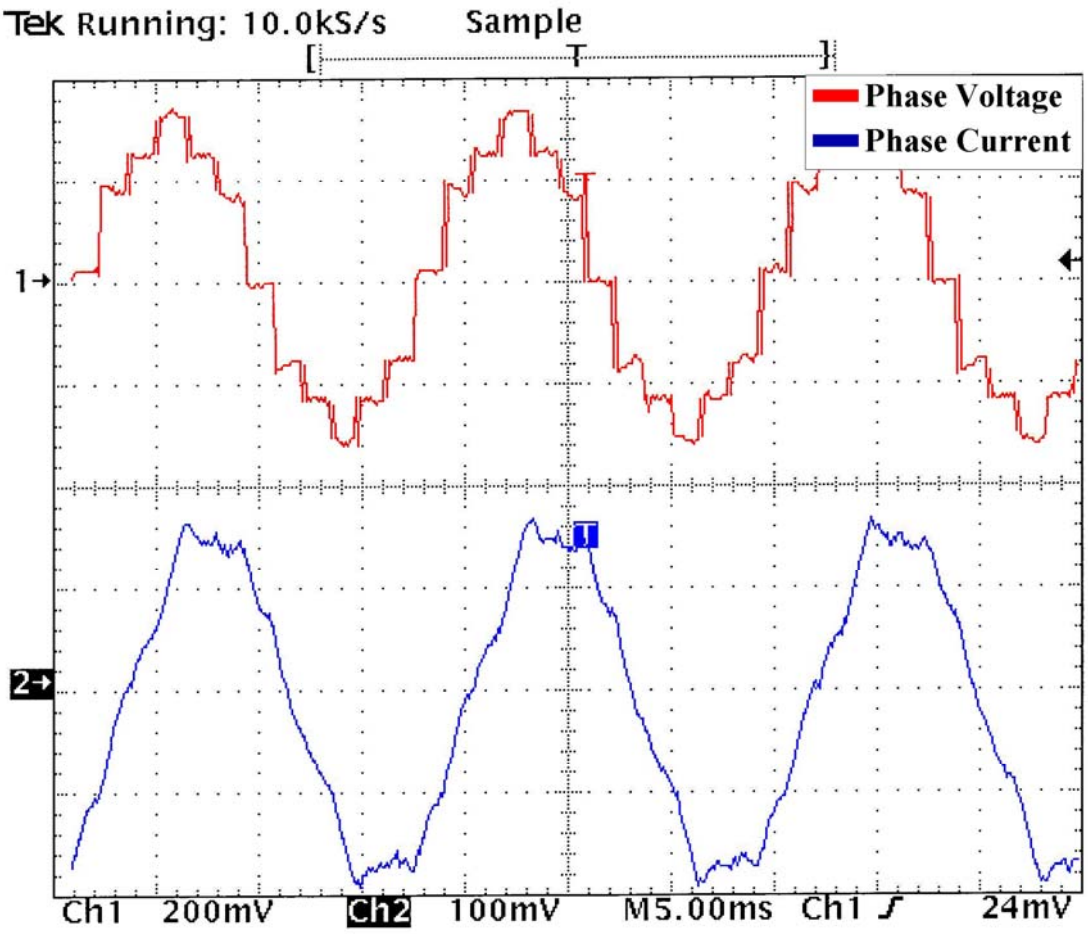

Figure 31. Phase Voltage and Current (Bulk Converter)

Figure 31 shows the phase voltage (red) and phase current (blue) waveforms for a single phase of the converter. The other phase voltage and current waveforms would look nearly identical. The differences between the three sets of waveforms would be slight variations in converter performance as well as being 120˚ out-of-phase.

Due to the use of a 1:500 voltage isolator and 1:1000 Hall-Effect current probe with a gain of 100, the actual scale for the voltage and current waveforms is 100 V/div and 1 A/div, respectively. It is important to note the peak amplitudes of the voltage and current waveforms. The peak amplitude for the voltage waveform is approximately 165 V. The peak amplitude for the current waveform is approximately 1.6 A. It is shown later that the peak amplitudes remain relatively unchanged when the conditioning converter is powered. This is due to the fact that the bulk converter is providing most of the power to the load.

The voltage waveform in Figure 31 is essentially a step approximation of a sine wave. The current waveform is a sine wave except with a high harmonic content. Figure 32 is a frequency-domain representation of the current waveform in Figure 31.

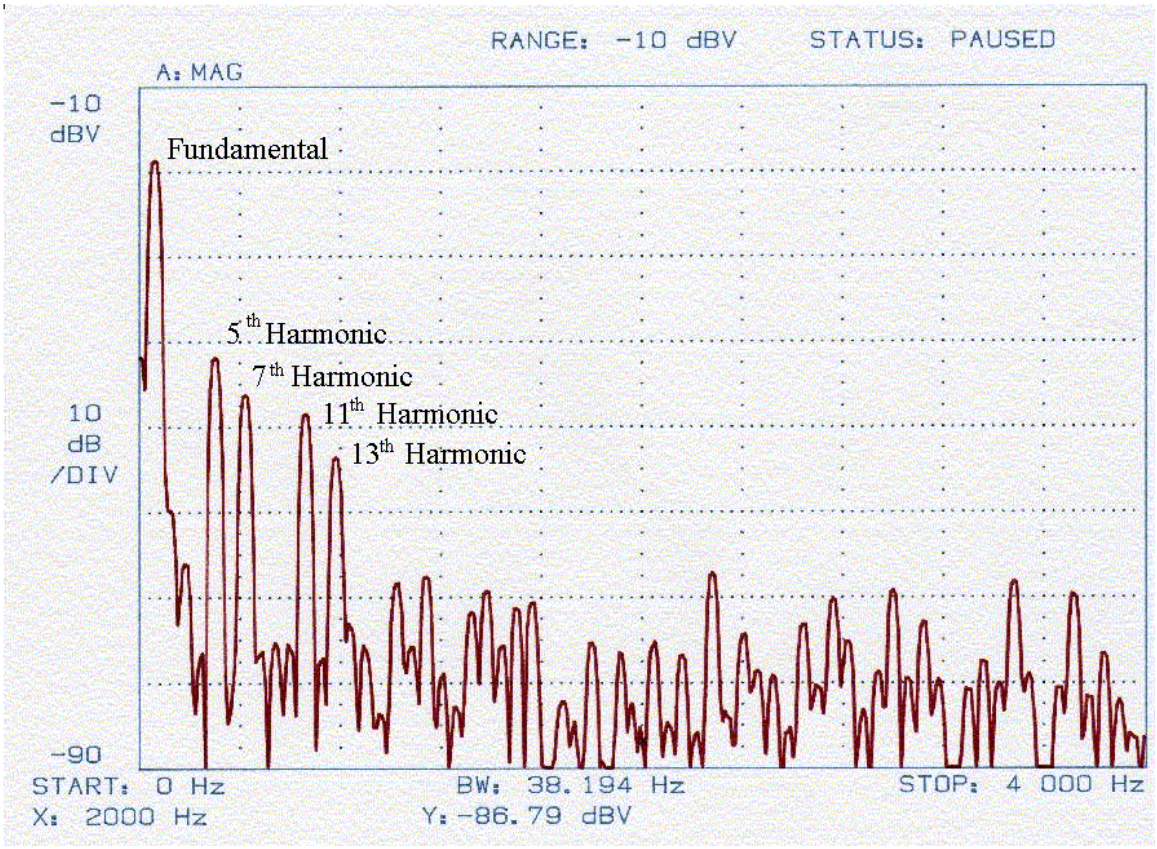

Figure 32. Frequency-Domain Representation of the Phase Current for Bulk Converter Operation only

The frequency-domain representation of a perfectly sinusoidal current would be one spike located at the fundamental frequency and no other spikes [7]. In Figure 32, the high harmonic content of the current waveform can be seen. The total harmonic distortion for the first 20 harmonics was measured to be 8.8%. Most notable of the harmonics are the 5^{th}, 7^{th}, 11^{th}, and 13^{th}. All four of these harmonics have a magnitude within 40 dB of the fundamental frequency's magnitude, with the highest being approximately 20 dB smaller than the fundamental frequency's magnitude. The goal of adding the conditioning converter is to remove the harmonic content of the phase current. The following section will discuss the results obtained from adding the conditioning converter.

2. Bulk and Conditioning Converter Testing

The second stage of testing consisted of operating the 3/3 CMLC as a cascaded converter. This means that both the bulk and conditioning converters were powered. As previously stated, the goal of this test is to reduce the harmonic content of the phase current. Figures 33 and 34 illustrate the result of this test.

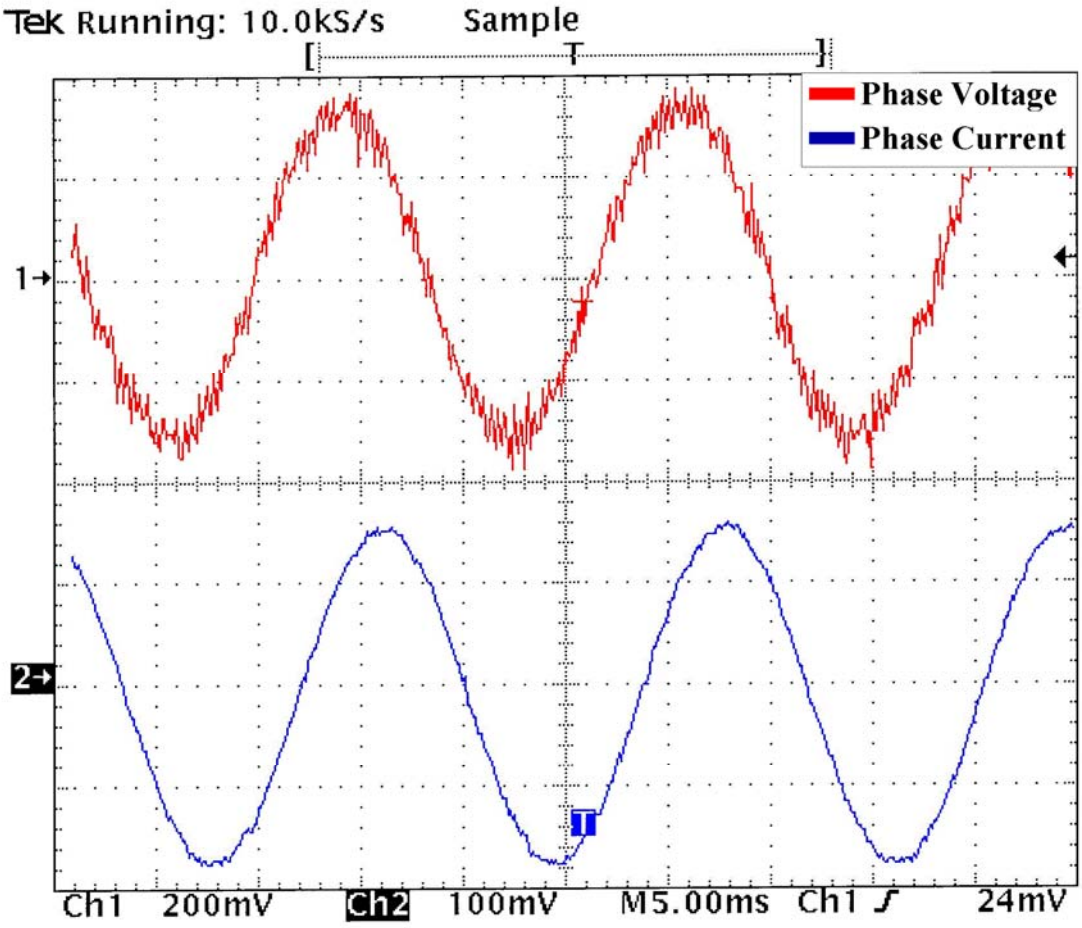

Figure 33. Phase Voltage and Current (Bulk and Conditioning)

Figure 33 shows the phase voltage (red) and phase current (blue) waveforms for a single phase of the converter. There is a significant difference between the waveforms in Figure 33 and the waveforms in Figure 31. The voltage waveform originally appeared to be a stepped sine wave, but now it appears to be nearly sinusoidal. The current waveform has had the harmonic content practically eliminated. However, the peak amplitudes for both the voltage and current waveforms have remained relatively unchanged. This leads to the conclusion that the bulk converter was in fact providing the majority of the power

to the motor load. The elimination of the current harmonics can be seen in Figure 34, which is the frequency-domain representation of the phase current.

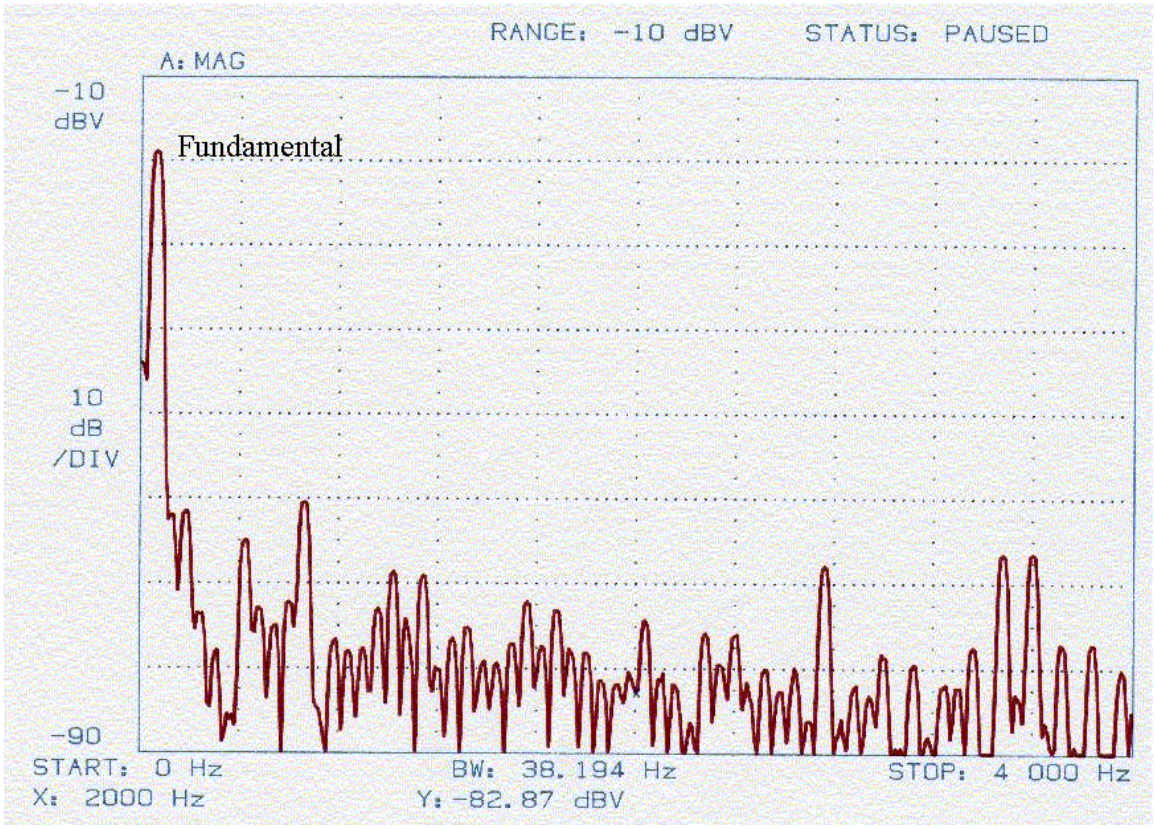

Figure 34. Frequency-Domain Representation of the Phase Current for Bulk and Conditioning Converter Operation

As can be seen in Figure 34, the harmonic content of the phase current has been suppressed. The four large harmonics that are clearly visible in Figure 32 have been significantly reduced in magnitude. All the harmonics for the entire spectrum are at least 40 dB smaller in magnitude than the fundamental frequency's magnitude. The total harmonic distortion of the first 20 harmonics was measured to be 1.3%.

In addition to ensuring that the conditioning converter was removing the harmonic content as designed, the three-phase performance of the cascaded converter was evaluated. Figures 35 and 36 show the phase voltages and currents, respectively.

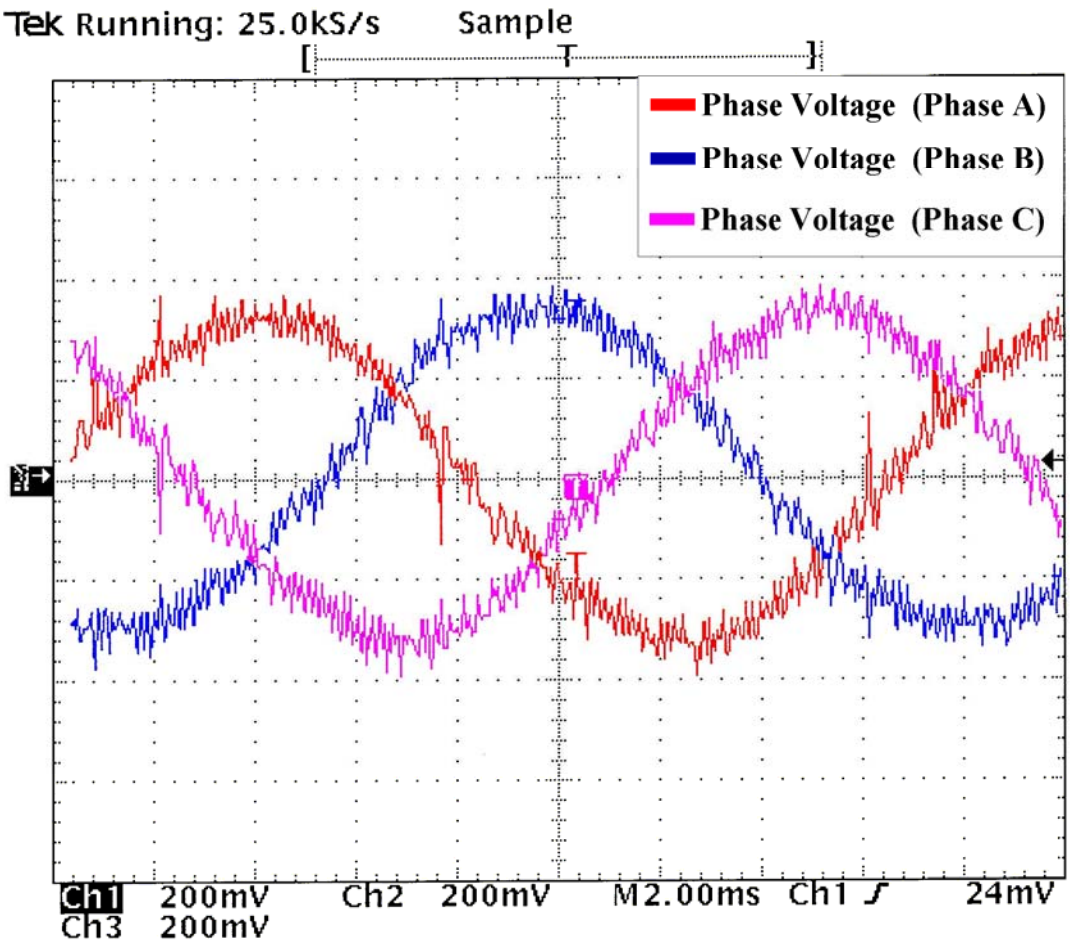

Figure 35. Phase Voltages (Three-Phase)

The phase voltages for the 3/3 CMLC should all be of the same amplitude and 120˚ out-of-phase. As can be seen in Figure 35, this relationship is clearly true. A similar relationship exists for the phase current waveforms.

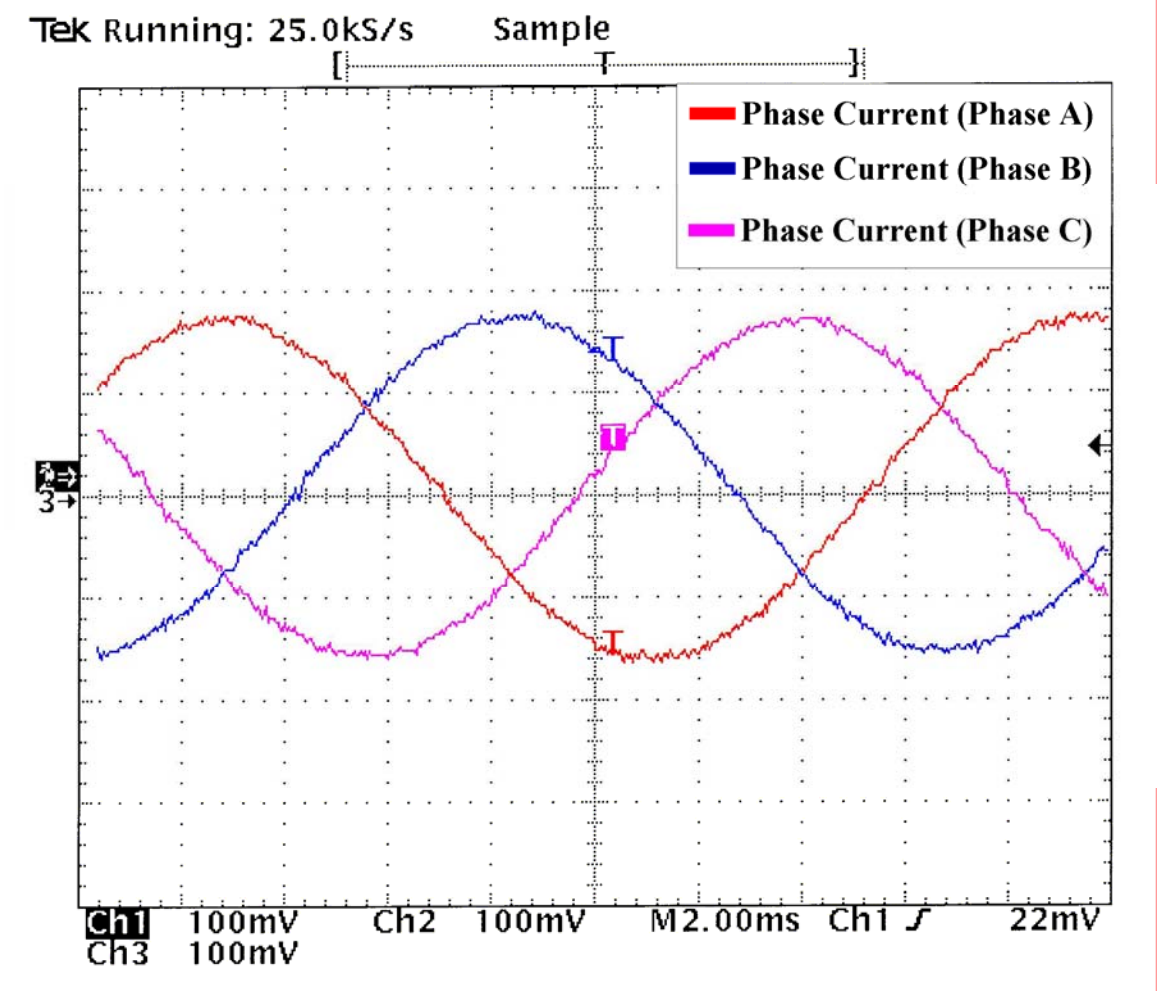

Figure 36. Phase Currents (Three-Phase)

As can be seen in Figure 36, the three phase currents have approximately the same amplitude and are in fact 120˚ out-of-phase with one and other. This means that the motor load is in fact a balanced three-phase load and that there is no zero sequence current.

The results obtained by testing the cascaded converter match the expected outcome. The reduction in harmonic content is clearly visible in both the time and frequency domains. Since reducing the current harmonics was the overall goal of this thesis, the tests were considered a complete success.

E. SUMMARY

Without the use of an advanced control algorithm, like the one developed for this thesis, the 3/3 CMLC constructed at NPS would never have been able to achieve such high fidelity current waveforms. The final testing of this converter with the SPWM control algorithm is considered a success. The overall THD was reduced from 8.8% to 1.3%. The following chapter will summarize the findings of this final performance analysis, provide some observations, and give suggestions for follow-on work.

VI. CONCLUSIONS

A. SUMMARY OF FINDINGS

The goal of this thesis was to develop an advanced control algorithm for a CMLC previously constructed in the Power Electronics Laboratory at NPS. The control algorithm chosen for this thesis was the SPWM algorithm. A DSP was used to interface the hardware converter with the control algorithm developed in Simulink.

After some design changes to the hardware portion of the converter, extensive testing was performed to ensure the algorithm worked properly. The results obtained during the final performance analysis are consistent with both the theoretical expectations and results obtained in similar research projects in universities throughout the United States.

The SPWM proved effective in reducing the THD of the output current when used to operate the bulk and conditioning converters. This reduction in harmonics was the major objective of this thesis.

This research will benefit future development of the all-electric ship designs already in various phases of construction and testing. Most notably of these programs is the DD(X). Since the DD(X) program uses a multi-level converter as the high power converter for the electric drive motor, this thesis can directly support development of a system to reduce the harmonic content of the phase currents.

B. OBSERVATIONS

The HIL design of the controller allowed for numerous changes to be made to the control algorithm developed for this thesis. These changes were easy to make and the results of the changes could be measured within minutes. The use of dSPACE and Simulink to build controllers for prototype converters should be encouraged since it is a quick and cost effective method for implementing controller designs.

Additionally, the results obtained using this method of control design are accurate and reliable. The lessons learned by interfacing hardware and software-simulations are invaluable. Many computer simulations simplify the system in order to make the simula-

tion development time reasonably fast. This simplification process means that either components are left out because they are too difficult to simulate or that the operation of the components is simplified in order to make them easier to simulate. With HIL simulation, there are no simplifications made because the hardware is physically connected to the simulation software.

The biggest problem encountered in this thesis was a flaw in the gate circuit design that allowed two or more switches to fire out of sequence, thus creating a bus short. While the problem was eventually corrected, this is an example of a situation that would be difficult to simulate because it relied on the response of actual hardware.

C. FUTURE WORK

The all-electric ship concept will be an integral part of future naval ship design. In order to remain a part of this revolution in ship technology, NPS should encourage follow-on work to this and similar theses. Possible areas for future research include:

- Development of a SVM controller.
- Comparison of SVM controller results with the results obtained in this thesis for the SPWM controller.
- Implementing the new gate driver design proposed in this thesis.
- Constructing a CMLC capable achieving more voltage levels.
- Constructing a higher power CMLC.

APPENDIX A

Appendix A contains the pin configuration table for the 50 pin digital I/O connector located on the CP1103 I/O board.

Pin	Connection	Pin	Connection	Pin	Connection
1	S1-A	18	S2-A	34	GND
2	S3-A	19	S4-A	35	GND
3	S1x-A	20	S2x-A	36	GND
4	S3x-A	21	S4x-A	37	GND
5	S1-B	22	S2-B	38	GND
6	S3-B	23	S4-B	39	GND
7	S1x-B	24	S2x-B	40	GND
8	S3x-B	25	S4x-B	41	GND
9	S1-C	26	S2-C	42	GND
10	S3-C	27	S4-C	43	GND
11	S1x-C	28	S2x-C	44	GND
12	S3x-C	29	S4x-C	45	GND
13	NC	30	NC	46	NC
14	NC	31	NC	47	NC
15	NC	32	NC	48	NC
16	NC	33	NC	49	NC
17	NC			50	NC

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF REFERENCES

[1] T. Doyle, H. Stevens, and H. Robey, "An historical overview of Navy electric drive," *Naval Symposium on Electric Machines*, Newport, RI, USA, July, 1997.

[2] United States Navy, "Navy Fact File – Aircraft Carriers," [http://www.chinfo.navy.mil/navpalib/ships/carriers/], last accessed June 2004.

[3] T.J. McCoy, "Powering the 21st-Century Fleet," *U.S. Naval Institute Proceedings*, Vol. 126/5/1.167, pp. 54–58, May 2000.

[4] M. Collins, "DD(X) IPS revolution in shipboard power," NAVSEA PEO-510 Internal Presentation, February 2003.

[5] Alstom, "Mermaid Pods," [http://www.alstom.com/static/html/acom-AGF_NavPage-NavPage_StandardLeft_1069324214761.html], last accessed June 2004.

[6] D. Finney, "AC motor variable frequency drives-consideration of the most economic and technically viable convertor power circuits for drives above 500 kW," *Proc. IEEE Colloquium on Very High Power Converter Devices and Applications*, pp. 6/1–6/4, December 1988.

[7] N. Mohan, T.M. Undeland, and W. P. Robbins, "*Power Electronics Converters, Applications, and Design*," pp. 442–445, John Wiley and Sons Inc., New Jersey, 2003.

[8] K.A. Corzine and J. R. Baker, "Multilevel voltage-source duty-cycle modulation: analysis and implementation," *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 5, pp. 1009–1016, 2002.

[9] K. A. Corzine, M. W. Wielebski, F.Z. Peng, and J. Wang, "Control of cascaded multi-level inverters," *Proc. IEEE Electric Machines and Drives Conference*, Vol. 3, IEEE International, pp. 1549–1555, 2003.

[10] R. Krishnan, "*Electric Motor Drives Modeling, Analysis, and Control*," pp. 209–212, Prentice Hall, New Jersey, 2001.

[11] F. Wang, "Sine-triangle vs. space vector modulation for three-level PWM voltage source inverters," *Proc. IEEE Industry Applications Conference*, Vol. 4, IEEE International, pp. 2482–2488, 2000.

[12] X. Kou, K.A. Corzine, and M. W. Wielebski, "Over-distention operation of cascaded multilevel inverters," *Proc. IEEE Electric Machines and Drives Conference*, Vol. 3, IEEE International, pp. 1535–1542, 2003.

[13] A.M. Hava, R. J. Kerkman, and T.A. Lipo, "Carrier-based PWM-VSI overmodulation strategies: analysis, comparison, and design," *IEEE Transactions on Power Electronics*, Vol. 13, No. 4, pp. 674–689, 1998.

[14] DSPACE, "Solutions for Control," Company Product Catalogue, 1997.

[15] DSPACE, "DS1103 PPC Controller Board," Company Technical Sheet, 2003.

[16] DSPACE, "Connector and LED Panels for Single-Board Hardware," Company Technical Sheet, 2003.

[17] R.A. Crowe, "Design, Construction and Testing of a Reduced-Scale Cascaded Multi-Level Converter," Master's thesis, Naval Postgraduate School, Monterey, California, 2003.

[18] A. S. Sedra and K. C. Smith, "*Microelectronic Circuits*," pp. 30–31, Oxford University Press, New York, 1998.

INITIAL DISTRIBUTION LIST

1. Defense Technical Information Center
   Ft. Belvoir, Virginia

2. Dudley Knox Library
   Naval Postgraduate School
   Monterey, California

3. Chairman, Code EC
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, California

4. Robert Ashton, Code EC/Ah
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, California

5. Jacob L. Barlow
   Monterey, California

6. Roberto Cristi, Code EC/Ah
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, California